Design of Power Efficient Timing Error Tolerant Circuit Using Clock Gating

Swarna Pragna,
M. Tech Student,
Department of ECE,
JNTUCEA,
Anantapur, Andhra Pradesh, India.

Abstract - *In order to avoid power and timing errors in the design, timing error tolerant circuits use clock gating. Timing issues are found and fixed with little logic by adjusting the flip-flop clock rather than the system clock. Because semiconductors experience errors frequently, timing inaccuracy is currently receiving more attention. Due to the newest semiconductor's high frequency and low supply voltage operation, even a minor external disturbance can jeopardise the timing margin between subsequent clocks. To reduce the power and Delay in the circuit using clock gating method and timing-error-tolerant method. The design and verify of schematic entry, circuit simulation, full- custom layout editing, placement and routing, netlist extraction, LVS and DRC verification of a circuit by Tanner EDA tool.*

***Key Words*: Clock gating, Tanner EDA Tool, Flip-flop, Timing error, Voltage**

1.INTRODUCTION

Multi-voltage/multi-frequency integrated circuits with nanometer technology and high complexity are reliability issues that are becoming more and more of a concern due to timing inaccuracies. In this study, a new bit-flipping flip-flop-based local error detection and repair algorithm is given. Timing issues are always corrected by complimenting the flip-output. flop's The timing-error rate increases together with the clock frequency. The circuit's critical paths are susceptible to timing issues since the clock period is reducing. Timing mistakes are very common in current integrated circuits due to the high incidence of Their performance is impacted by CMOS process, power supply, and temperature changes. As the supply voltage falls, the delay of the circuit might drastically change between the best and worst process, voltage, and temperature (PVT) conditions. Process variability in device and circuit characteristics is one of the key problems the semiconductor industry is now facing. Timing errors very frequently occur as a result of transistor ageing problems. The negative-bias temperature instability (NBTI) of CMOS lowers the threshold voltage, which lengthens the logic paths. A timing-error-tolerant methodology is essential for building reliable systems. A system's capacity to continue operating even after experiencing an error is known as error tolerance. In other words, an error-tolerant system is one where faults are largely innocuous in terms of their effects. Dynamic parameter variation, brought on by changes in the environment and workload, is also possible when the chip is operating in addition to static variations that happen during chip production. Dynamic variations include things like temperature changes, supply voltage drops, and transistor ageing degradation. If not managed properly, variations can negatively affect performance, power, and the system's overall reliability because they alter the timing and power consumption characteristics of the circuit.

2. LITERATURE SURVEY

2.1 Literature Review Paper - 1

Title: "A Wide-Voltage-Range Half-Path Timing Error-Detection System With a 9-Transistor Transition-Detector in 40-nm CMOS" IEEE Transactions on Circuits and Systems I, Volume: 66, Issue: 6, June 2019

Authors: Weiwei Shan, Xin Chao Shang, Xing Wan, HaoCai, Chaun Zhang, Jun Yang.

Outcome: The authors proposed A half-path insertion point selection method so that the timing errors in the For the purpose of avoiding actual timing mistakes at the endpoints, the current clock cycle can be recognised beforehand.

2.2 Literature Review Paper – 2

Title: "A Low-Power Timing-Error-Tolerant Circuit by controlling a clock"March 2021, IEEE Transactions on Very Large-Scale Integration (VLSI) Systems, Volume 29, Number3 .

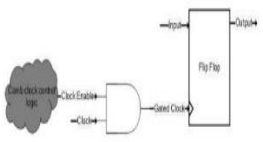
Authors: Isaak Yang and Kwang-Hyun Cho

Outcome: The authors proposed a circuit that is time borrowing capable and is timing error tolerant, allowing it to quickly repair timing errors while maintaining a small circuit size. By using this method, the average power consumed 3.814682 mwatts.

3. ARCHITECTURE

Clock Gating Method: Many synchronous circuits employ the power-management method known as clock gating to dynamic power dissipation, by removing the clock signal when the circuit is not in use or ignores the clock signal. By cutting down the clock tree, clock gating reduces power consumption at the expense of increasing the amount of logic in a circuit.

Fig 1 : Clock gating method



3.1 Timing error tolerant circuit by using Clock gating Method: Method that is timing-error-tolerant and has a quick mechanism for fixing timing errors. By managing the clock's transparent window, it is possible to identify and fix timing errors that result in unexpected data transitions after the rising edge of the clock in the critical path. With the fewest possible logics, the timing error is directly fixed. Additionally, we introduce our time-borrowing technique, which handles successive faults. When timing errors happen in two stages back-to-back, the second stage's modified CLK keeps a transparent window open for long enough to allow for the storage of regular data without modifying the system CLK.

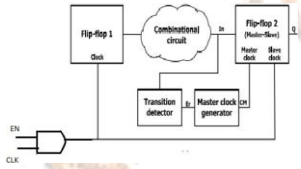


Fig 2 : Timing error tolerant circuit using clock gating method

3.1 Combinational logic circuit: The circuit which The current combination of inputs determines the output. Logic gates are the building blocks of combinational circuits. The logic function determines each logic gate's output.

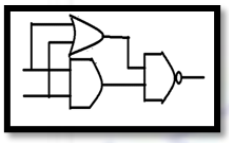


Fig 3: Combinational logic circuit

3.2 Transition Detector: Transition detector is used in flip-flops in order achieve edge triggering in the circuit

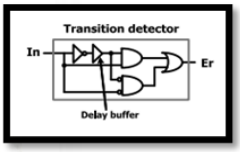


Fig 4: Transition Detector

3.3 Master clock generator: The gadget that sends the clock signal to the gadgets so they can synchronise is called a master clock generator. The associated equipment is referred to as a "slave," and it is this group of clocks that is synced with the master clock to form the clock network.

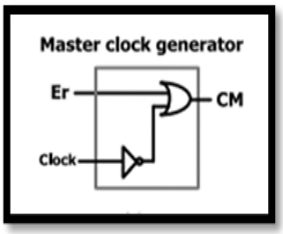


Fig 5: Master clock generator

4. TANNER EDA TOOL

Pre-fabrication verification is a significant element a phase of the design process used to create electronic circuits. Accurate verification is essential to effective design due to the costs and time constraints involved with the fabrication stage. In order to design and test a circuit's functionality, an EDA tool must solve the differential equations characterising the circuit numerically. Before submitting their ideas for production, circuit designers can validate and fine-tune them using the results of the simulation. Tanner EDA tool is a fully functional circuit design and analysis solution that offers the following features:

4.1 Schematic Editor (S-Edit): With the help of the potent design capture and analysis tool schematic editor, netlists for use in T-Spice simulations can be created. A user-friendly PC-based design environment for schematic capturing is called Schematic Editor (S-Edit). It gives you the strength you need to manage your most challenging full custom IC design capture.

4.2 Pre layout simulation: After creating the schematic, you must determine whether your design adheres to the specifications. For this reason, you must perform pre-layout simulation, which simulates the design.

4.3 T-Spice Circuit Simulator: Simulating analogue and hybrid analog/digital circuits with T-Spice is quick and precise. The simulator features linked line models, the most recent and best device models on the market, as well providing assistance for user-defined gadget models via C functions or tables. All commercially available SPICE simulation applications are compatible with T- Spice's enhanced SPICE input language. All of SPICE's device models are included, along with resistors, capacitors, mutual inductors, single and linked transmission lines, current sources, voltage sources, controlled sources, and the most recent sophisticated Berkeley and Philips Labs' models of semiconductor devices.

4.4 Waveform Editor(W-Edit): Displayed by W-Edit Waveforms produced by the T-Spice simulation as it is run. for the purpose of evaluating, comprehending, and enhancing VLSI circuits, it is essential to visualise the complex numerical data generated by the simulations. In a customizable framework created for graphical data presentation, A waveform viewer with power, speed, and simplicity is W-Edit.

4.5 Layout Editor (L-Edit): Tanner EDA tool contains Standard LVS for layout versus schematic, Interactive DRC for real-time design rule verification while editing, Typical DRC for a hierarchical DRC, Typical Extract for netlist extraction, and Standard L- Edit for layout editing.

5. SCHEMATIC CIRCUIT

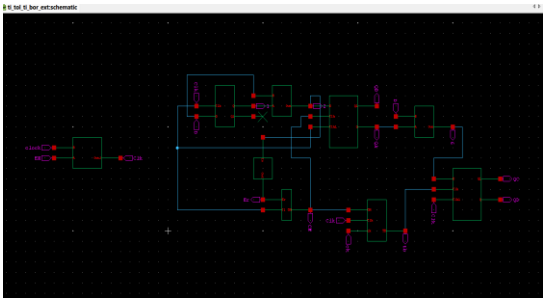


Fig 6: Schematic circuit of Timing error tolerant circuit by using Clock gating Method

6. RESULTS

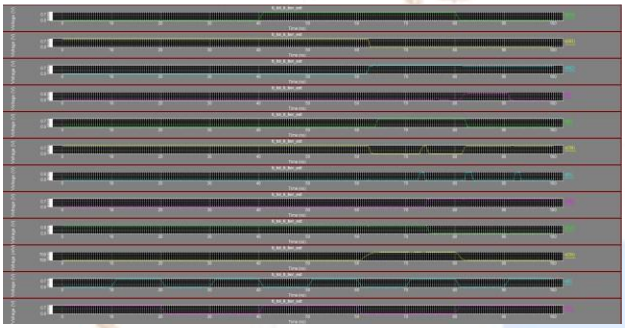


Fig 7: Proposed Result

7. POWER/DELAY REPORT

	Power	Delay
Existing	3.841682 mW	72.098 ns
Implementation	1.343312 mW	41.818 ns

8. CONCLUSION

In this article, we propose a timing error tolerant circuit using clock gating method and that can correct and reduce a timing error and power immediately with a compact circuit structure. We have presented an effective method using clock gating and a timing error tolerant circuit, to detect and fix timing and power issues. Clock gating method reduce dynamic power dissipation, by removing when the circuit ignores or is not using the clock signal. aberrant data are present in the crucial path. Controlling the transparent clock window allows for the detection and correction of transitions that occur after the clock's edge. A minimal number of logics directly repair the timing problem.

9. REFERENCES

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