DESIGN AND IMPLEMENTATION OF LOW POWERCOUNTERS USING REVERSIBLE LOGIC GATE

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***Abstract*— Due to its low power usage, the reversible logic design garners increasing attention. Numerous studies have been conducted on both sequential and combinational reversible circuitdesign. Utilizing reversible logic is one approach to power optimization. It can be applied to optical computing, quantum computing, nanotechnology, and low power CMOS designs.**
Keywords—Reversible Logic Gates, Feynman Gates, Fredkin Gates, Power Synthesis.

I. INTRODUCTION

Reversible computations have the ability to generate inputs from outputs, pause, and travel back in time to any previous computation step. If the input vector can be clearly recovered from the output vector and there is a one-to-one correspondence between the circuit's input and output assignments, then the circuit is said to be reversible. In other words, not only can the outputs be clearly determined from the inputs, but the inputs can also be recovered from the outputs.

Energy dissipation is decreased or perhaps completely eliminated in information-lossless computation. According to Landauer, every piece of data that is lost or distorted during computing generates a significant amount of heat energy, which may be expressed in Joules as the product of the Boltzmann's constant (K), the absolute temperature (T).

Loss of information causes high-frequency signals to generate and dissipate additional heat energy. Bennett also demonstrated that if the procedures are carried out in a reversible manner, the resulting power dissipation can be greatly decreased. It explains the idea of reversible logic, which states that a circuit can reverse at any time to retrieve adata bit. As a result, no information is actually lost, and the heat produced is likewise extremely small.

II. MOTIVATION

In digital communication systems, VLSI technologies are essential, and energy dissipation is crucial to IC technology. Conventional digital systems have considerable energy dissipation in every logical computation, which results in information loss in every transition.

Because of loss of information during the operation, the ordinary logic gate generates heat, necessitating theintroduction of reversible logic. There is currently no physical means to increase performance, so reversible circuits that retain information by uncomputing bits rather than discarding them will soon be the only option. Reversible computing will also result in increased energy efficiency, which will accelerate nanoscalecircuits and, by extension, most computing applications.

III. PROBLEM STATEMENT

A memoryless logic component known as a reversible logic gate implements an injective logical function. Typical ones are Fredkin gates, Toffoli gates, interaction gates, and switch gates.

The gates with the attribute of having an equal number of inputs and outputs, or n inputs and n outputs, are known as reversible gates or reversible logic gates. The amount of energy lost during computations will be minimised when the number of inputs and outputs is equal.

Therefore, we can apply reversible logic technology to increase rapidity, reduce energy dispersion, and dissipate heat. As a result, it is employed to increase speed and decrease energy usage.

IV. OBJECTIVES

Although reversible computing may have applications in transaction processing and computer security, its greatest long-term advantages will be realised in fields that demand high levels of speed, performance, and efficiency. It comprises the region.

•Lower operating expenses.
• Reduce the need for cooling and to lessen noise.
• To lower energy and cooling operational expenses.
Why battery energy consumption won't increase significantlyin the foreseeable future for technological and safety reasons
• Low-power data paths and arithmetic designs for digital

signal processing (DSP)
• Field Programmable Gate Arrays (FPGAs) in CMOS technology for incredibly low power consumption, great testability, and self-repair.

V. RELATED WORK

Reversible gates of the Toffoli type are examined. The first Peres-type ternary gates are presented. Since the first quantum computers were made available via the Internet today, reversible and quantum computing have seen significant advancements in the binary domain.

Lemma 1: A matrix is self-inverse if it is both orthogonal and symmetric.
Lemma 2: A pair of unitary matrices' product is also unitary. Polarities and quantum models - A gate will be referred to asbeing controlled if the value of one or more control signals affects how well it performs.

In one of the papers, Wavelet transforms have become one ofthe most useful classes of transforms, and they are used in a variety of industries, including orthogonal frequency division multiplexing, machine learning, sound analysis, imageprocessing, and video processing.
To get two level 2-D 2 2, one level 2-D 4 4, and two level 2- D 4 4 Haar transforms, the above designs can be combined. The suggested designs are QC, CI, GO, and GC optimised. Additionally, this study suggests two approximate adders thatare optimised for systems based on reversible logic.

The reversible computing paradigm is gaining popularity (especially for so-called emerging technologies), and it serves as the foundation for many applications, such as quantum computation, some low-power design considerations, the design of adiabatic circuits, interconnects, encoding and decoding devices, and verification.
Both a fundamental VHDL code realisation and some suggestions for enhancing circuit measures have been explored. The proposed method has been contrasted with an exclusive reversible HDL method that makes use of the SyReC language.
Reversible circuits that can carry out intricate logical and mathematical operations are created by combining reversible gates. The realisation of one-to-one mapping between inputsand outputs takes place. This study examines the design and evaluation of the following reversible logic gates: the Feynman gate, the Peres gate, the modified Fredkin gate, andthe modified Toffoli gate.
Instead of employing planar MOSFETs, reversible circuits can be created using multigated MOSFETs, Tunnel FETs, etc. Multi-gated MOSFETs can greatly minimise the short channel effects, power dissipation, and latency of the logic circuits due to better electrostatic control.
Comparative analysis is done on a number of characteristics,including quantum cost, garbage output, gate count, anddelay of various reversible gates and various circuits. Additionally, comparisons of power and surface areaoccupancy between current circuits and traditional ones havebeen done.
Reversible logic enables the system to be operated both forward and backward. Reversible circuits are designed primarily to reduce hardware complexity, the number of reversible gates, garbage outputs, constant inputs, quantum cost, area, power, and latency.
A comparison of numerous reversible logic gates is revealed in this research. The article offers a few reversible logic gates that can be used to create more intricate systems with reversible circuits and to carry out more challenging tasks onquantum computers.

Reversible sequential circuit design was one attempt. This project uses a reversible T Flip-flop to create designs for an asynchronous counter. The designs of the counters have usesin the construction of reversible processors, reversible Johnson & ring counters, reversible ALUs, and reversible processors.

The literature review and fundamental definitions of reversible logic are presented about reversible logic gates, how they are implemented, and provides a comparison Techniques for minimizing dynamic, leakage, and short circuit power consumption are used in logic design. At different abstract levels, CPU power optimization is possible.

VI DESIGN METHODOLOGY

A. Counters

Numerous flip-flops connected in cascade make up a counter circuit.
The usage of counters in digital circuits is fairly widespread. They can be produced as standalone integrated circuits or as a component of larger integrated circuits. Counter is a digital circuit which is used to countpulses. The most widespread use of flip-flops is on counters.

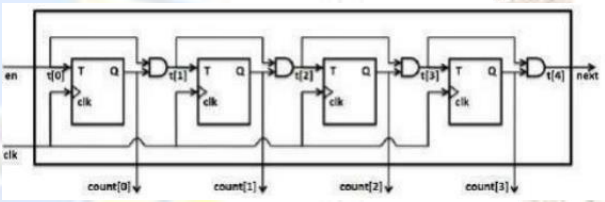

Figure 6.1 Counter

Synchronous Counter, the external clock signal is connected to the clock input of every individual flip-flop within the counter so that all of the flip-flops are clocked together simultaneously (in parallel) at the same time giving a fixed time relationship as shown in Figure 4.1.

B. Reversible Logic

Researchers are interested in reversible computing because it uses less energy and generates less heat. Different scholars have offered a variety of reversible gates, and they have also suggested a variety of combinational circuits based on reversible gates. Heat dissipation is growing in importance as digital circuit complexity rises. R.Landauer demonstrated in the early 1960s that information loss caused by reversible hardware computation results in energy loss. It had demonstrated that every piece of information lost causes at least KTLn2 joules of energy to be lost. It is well knowledge that everyoperation involving an irreversible gate erases at least onepiece of data. Therefore, some heat energy will always beproduced by these gates.

6.3 Reversible Logic gates

A reversible gate is a circuit in which the number of outputs is equal to the number of inputs and the input and output vectors correspond one to one. Garbage output is the unwanted or unused output of a reversible gate or circuit. Reversible logic gates include the Feynman, Fredkin, Peres, and Toffoli gates, among others.

Feynman Gate

Feynman gate is a 2*2 one through reversible gate as shown in Figure 6.2. The input vector is I(A, B) and the output vector is O (P, Q).

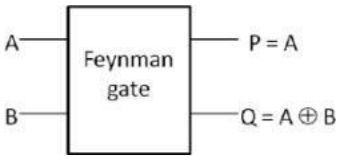

Figure 6.2 Feynman Gate Block diagram

Input		Output	
A	*B*	*P*	*Q*
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Figure 6.3 Feynman Gate Truth Table

Feynman gate is also recognized as controlled- not gate (CNOT). It has two inputs (A, B) and two outputs (P, Q).The outputs are defined by P = A, Q =A XOR B As shownin the truth table Figure 6.3.This gate can be used to copy a signal. Since fan-out is not allowed in reversible logic circuits, the Feynman gate is used as the fan-out gate to copy a signal.

Toffoli Gate

It is invented by Tommaso Toffoli, is a universal reversible logic gate, which means that any reversible circuit can be constructed from Toffoli gates. It is also known as the "controlled-controlled-not gate, which describes its action. It has 3-bit inputs and outputs; if first two bits are set, it inverts the third bit, otherwise all bits stay the same as shown in table Figure 6.4 and 6.5 shows the block diagram of Toffoli gate

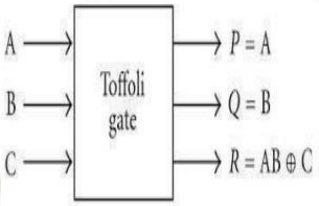

Figure 6.4 : Toffoli Gate Block Diagram

A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Figure 6.5: Toffoli Gate Truth tableFredkin Gate

Fredkin Gate

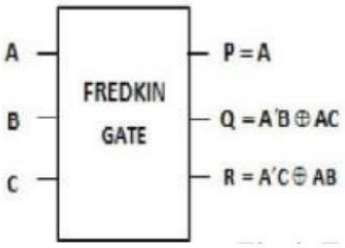

Figure 6.6 : Fredkin Gate Block Diagram

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	0	1
1	1	0	1	1	1
1	1	1	1	1	0

Figure 6.7: Fredkin Gate Truth Table

The Fredkin gate is a circuit or device with three inputs and three outputs that transmits the first bit unchanged andswaps the last two bits if, and only if, the first bit is 1. Thebasic Fredkin gate is a controlled swap gate. The truth table of Fredkin gate is as shown in table Figure 6.7 and Figure 6.6 shows the block diagram of Fredkin gate.

Sayem Gate

Sayem gate is a 4*4 reversible gate and is used in designing sequential reversible circuits. The input and output vector of this gate are 1v = (A,B,C,D) and 0v = (A,A'B+AC,A'B+AC+D,AB+A'C+D)

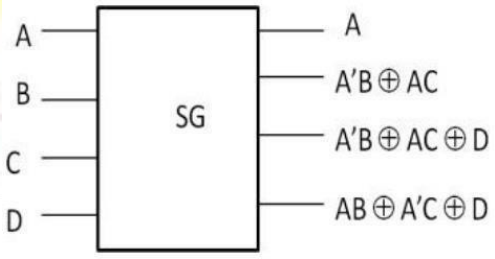

Figure 6.8 : Sayem Gate Block Diagram

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	1
0	0	1	0	0	0	0	1
0	0	1	1	0	0	1	0
0	1	0	0	0	1	1	0
0	1	0	1	0	1	0	1
0	1	1	0	0	1	1	1
0	1	1	1	0	1	0	0
1	0	0	0	1	0	0	0
1	0	0	1	1	0	1	1
1	0	1	0	1	1	1	0
1	0	1	1	1	1	0	1
1	1	0	0	1	0	0	1
1	1	0	1	1	0	1	0
1	1	1	0	1	1	1	1
1	1	1	1	1	1	0	0

Figure 6.9 : Sayem Gate Truth Table

The block diagram and truth table are as shown in theFigure 6.8 and Figure 6.9.

T FLIP-FLOP

The block diagram of T-flip flop is as shown in Figure 6.10.T-flip flop toggles the output when the input is high and retains the output when the input is low, thus it does two operations, and it either holds the last state or toggles the output. The T flip-flop is also called toggle flip-flop. It is a change of the JK flip-flop. The T flip flop is received by relating both inputs ofa JK flip-flop. The truth table of T-flip flop is as shown in fig6.11.

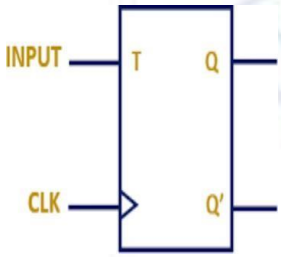

Figure 6.10 : T Flip Flop Block DiagramFigure

T	Clock	Q	Q'
0	↑	Q	Q'
1	↑	Q'	Q
X	↓	Q	Q'

6.11 :T Flip Flop Truth Table REVERSIBLE T FLIP FLOP USING TOFFOLI GATE

Reversible T-flip flop can be built by using 3x3 Toffoli gate, which as two garbage output and T-flip flop output. Toffoli gate is designed as shown in figure 6.12 which performs one REVERSIBLE LOGIC operation of T-flip flop.

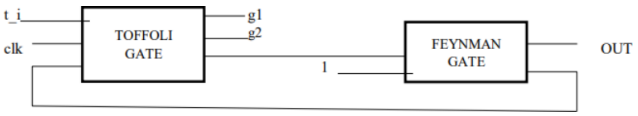

Figure 6.12 Reversible T Flip Flop using Toffoli Gate

Each input of Toffoli gate is mapped to each output. Toffoli isa universal reversible logic gate which means that any reversible circuit can be constructed from Toffoli gates. It is also known as "controlled-controlled NOT" gate which describes its action.

REVERSIBLE T FLIP FLOP USING FREDKIN AND FEYNMAN GATE

Reversible T-flip flop can be built using Fredkin gate and Feynman gate as shown in Figure 6.13 which performs same operation as that of normal T-flip flop. The design uses two Fredkin gate and two Feynman gate to perform operation like T-flip flop. It has three 3 Garbage output in the design.

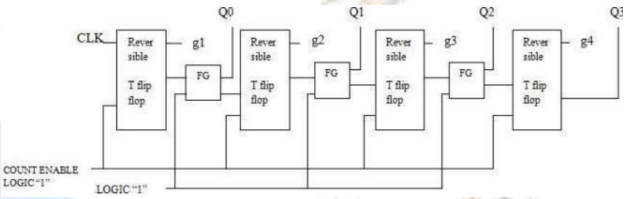

Figure 6.13Reversible T flip flop using Fredkin and Feynman gate.

REVERSIBLE 4-BIT ASYNCHRONOUS COUNTER

A counter's primary purpose is to count the sequence ofinput pulses supplied to it in digital form. It consists of aset of flip flops coupled in a proper manner.

The output transition of one flip-flop server serves as asource for activating other flip-flops in asynchronous counters. Toffoli gate, for example.

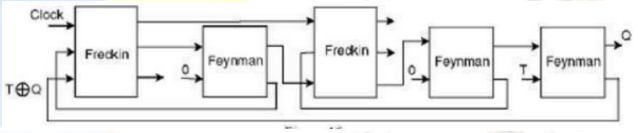

Figure 6.14: Reversible 4-Bit Asynchronous counter

At the output of each reversible T flip flop the Feynman gate is used for complemented Q output with the input B-

1. These complemented Q output of each Reversible T-flip flop trigger the subsequent Reversible Tflip flop andreversible design performs the up-counter operation as shown in Figure 6.14.

VI. SPECIFICATIONSSOFTWARE DETAILS

Software created by Xilinx for the synthesis and analysis of HDL Design is known as Xilinx ISE (Integrated Synthesis Environment).

Cadence The enhanced parasitic estimating and comparison flow and optimisation algorithms available to designers through Virtuoso enable to better centre designs for yield improvement as well as advance matching and sensitive analysis.

HARDWARE DETAILS

FPGA (Field Programmable Gate Array) hardware isutilized. Programmable Read-Only Memory (PROM) and Programmable Logic Devices (PLD) were the ancestors of the FPGA business. Both PROMs and PLDs had the ability to be programmed. Programmable Read-Only Memory (PROM) and in the field (field programmable) gave rise to the FPGA business.

VII. RESULTS

File: /home/cadence/DATABASE/counter/counter_p1

Instance: /updowncount
Power Unit: W
PDB Frames: /stim#0/frame#0

Category	Leakage	Internal	Switching	Total	Row%
memory	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
register	5.33792e-10	2.08729e-07	1.94400e-08	2.28703e-07	61.36%
latch	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
logic	4.37375e-10	1.08467e-07	3.50980e-08	1.44003e-07	38.64%
bbox	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
clock	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pad	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pm	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
Subtotal	9.71167e-10	3.17197e-07	5.45380e-08	3.72706e-07	100.00%
Percentage	0.26%	85.11%	14.63%	100.00%	100.00%

Fig 7.1 : Counter power report

Instance: /svs
Power Unit: W
PDB Frames: /stim#0/frame#0

Category	Leakage	Internal	Switching	Total	Row%
memory	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
register	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
latch	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
logic	2.24774e-10	7.30823e-08	2.99700e-08	1.03277e-07	100.00%
bbox	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
clock	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pad	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pm	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
Subtotal	2.24774e-10	7.30823e-08	2.99700e-08	1.03277e-07	100.00%
Percentage	0.22%	70.76%	29.02%	100.00%	100.00%

Fig 7.2: SVS power report

Instance: /four_bit
Power Unit: W
PDB Frames: /stim#0/frame#0

Category	Leakage	Internal	Switching	Total	Row%
memory	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
register	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
latch	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
logic	7.17848e-10	3.45075e-07	8.21370e-08	4.27930e-07	100.00%
bbox	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
clock	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pad	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
pm	0.00000e+00	0.00000e+00	0.00000e+00	0.00000e+00	0.00%
Subtotal	7.17848e-10	3.45075e-07	8.21370e-08	4.27930e-07	100.00%
Percentage	0.17%	80.64%	19.19%	100.00%	100.00%

Fig 7.3: Toffoli Power repor

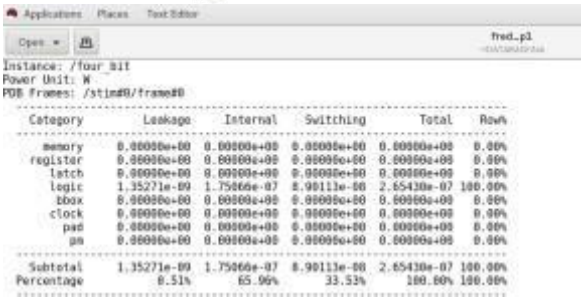

Fig 7.4: Fredkin power report

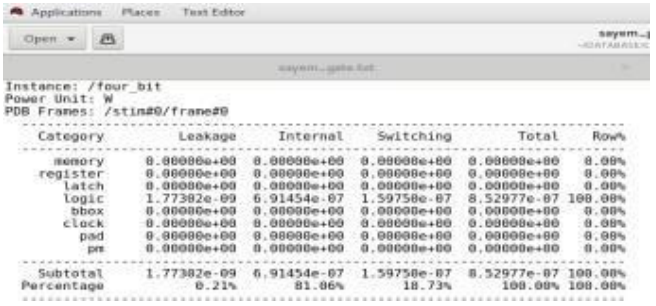

Fig 7.5: Sayem power report

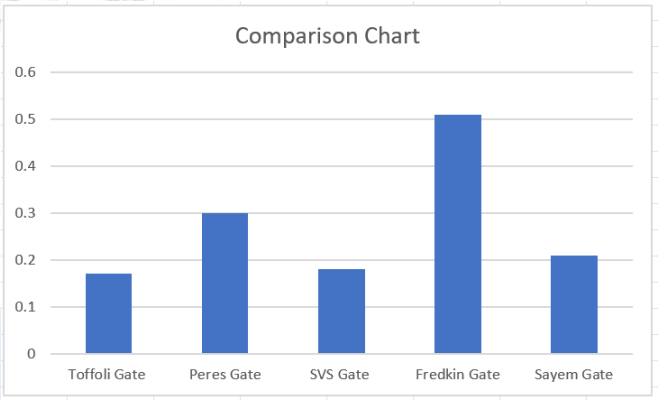

Fig 7.6 Comparison Chart

The fig 7.6 shows the comparison chart of percentage of powers of different gates. Toffoli Gate is proved to be the best with respect to power dissipation.

VIII. CONCLUSION

Low power CMOS VLSI design is particularly interested in reversible circuits. Logically irreversible circuits experience information loss during operation, which is actually translated into heat. Therefore, information loss causes powerto be lost. Toffoli gate is used in an asynchronous up-counterusing a reversible T-flip flop because it has less power dissipation than other gates like the SVS gate, Sayem gate, and Fredkin gate. Because of this, it is observed that Toffoli gate has less power dissipation than other designed reversibleT-flip flops. As a result, it is more efficient than other designed gates. When compared to the current model, the power consumption is lowered, and the reduction is also shown in the gate delay, garbage outputs, delay, and quantum cost. The intricacy of the hardware is another crucial factor. The process of operating the system both forward and backward is supported by reversible logic. Reversible computations can therefore produce inputs from outputs, halt, and then resume at any point in the computation's history.

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