Low Power Digital Circuit Design using Asynchronous Logic

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Abstract - In this paper, a novel technique for obtaining low power is presented. It involves lowering the design's reliance on the clock signal. Although a clock signal uses power even when the circuit is not in use, asynchronous circuits automatically transition into the no transition occurs in the circuit during the idle state. Additionally, in an active system, power is only lost by the components that are actually being used. The main goal of this effort was to leverage asynchronous logic to implement low power. By creating a straightforward Display Controller, the researchers also investigated how power consumption utilizing asynchronous logic is measured. The investigation also investigated the trade-offs between asynchronous design's complexity, size, and power requirements. The asynchronous design used around 17% less power than its synchronous version when the power consumption of the synchronous and asynchronous display controllers was measured. The asynchronous design took up twice as much space as the synchronous one. By using asynchronous logic, the dependency of the design on the clock signal can be decreased.

I. INTRODUCTION

(1) Need for Low Power Design

Many variables, including the emergence of portable devices, heat considerations, reliability challenges, and, lastly, environmental concerns, drive the demand for low power design. The most significant element driving the requirement for low power design is the emergence of portable or mobile communication devices like laptops, cell phones, video games, etc. The demand for portable computers is expected to continue to rise in the coming years [1]. The advancement of low power circuit design is clearly in the interest of the economy as consumers seek out powerful but power-efficient products. The need for low power dissipation and high throughput in various portable devices and their applications is the main driver behind the development of low power circuits. Consequently, low power digital design.

(2) An Introduction to Asynchronous Design

By lowering the amount of switching events required to complete a task, low power digital system design can be achieved at different levels, including the process, circuit, architectural, and algorithm levels. The design level of the method that can be used to lower power dissipation in digital integrated circuits will be the main focus of this thesis. The majority of modern digital integrated circuits are synchronous in nature. In synchronous circuits, a clock signal that is dispersed across the circuit establishes a single time for all components [12]. As the clock frequency rises in high-speed circuits, power usage also rises progressively. Reducing the circuit's reliance on the clock signal is an efficient way to lower power usage. In order to do this, the Asynchronous design, in contrast to conventional device design, lacks a centralized clock, which is used to coordinate data progress. When the current step of the design is finished, a pipeline controller logic initiates the following stage. This guarantees that A central clock is not required. Without waiting for the central clock, the device's components can operate at various rates [10]. Additionally, even when a system is not in use, the clock signal uses a significant amount of chip power.

Asynchronous circuits have the benefit of entering an idle state by nature; during this state, there won't be any transitions in the circuit. So, by choosing asynchronous logic, electricity is only used for productive purposes. Another positive The fact that, even in an active system, only the subsystem required for processing would dissipate power has an impact on asynchronous design [13]. As a result, power that would have been used to generate a clock signal is spared. Additionally, it is possible to safely lower the supply voltage, either statically or dynamically, to match the actual throughput to the required computation rate, which will result in power savings [11]. Synchronous design creates sophisticated circuitry to accelerate rare, worst-case conditions in order to meet timing requirements. In turn, more power is used as a result. When using an asynchronous design, worst-case operations can move slowly while making use of the resources and power usage of routine activities [11]. Due to the observation that synchronous logic has started to hit its limits, asynchronous logic has started to garner attention. Global synchronization gets challenging and clock skew becomes an issue as transistor count rises. As opposed to synchronous logic, which experiences problems with global synchrony and clock skew, asynchronous logic generates local timing signals [11].

II.GLOBALLY ASYNCHRONOUS LOCALLY SYNCHRONOUS (GALS) DESIGN

The clock signal has a number of uses in synchronous systems. The clock signal is a universal signal. The flip-flops are updated during the clock edge, and the new state propagates throughout the circuit to determine the following state. This offers a selection of structured design techniques. The replacement of the world clock by a timing discipline is necessary for the systematic design of asynchronous circuits. For this, straightforward request and acknowledge signalling can be applied. While the component on the receiving side waits and acknowledges, the subsystem on the transmitting side actively participates in the transition. This is known as shaking hands. The handshake latch and the transferrer are the two handshake components used in data-paths the most frequently. The handshake latch works similarly to The energy needed for a handshake latch's write operation is 2 or 4 transitions, while the energy needed for its read operation is 4 transitions [14]. Energy is not needed for the transferrer to function. The section modulus increased by 25 percent to actual for bending

Asynchronous design increases chip area while consuming less power. Due to the added cost of extra circuits for handshaking and a larger routing region, this is the case. The circuit can be tolerant to variations in delay thanks to asynchronous architecture. The speed independent and delay-insensitive models can function even when there are delays in the interconnects and gates. These techniques demand a lot of engineering time and have quite sophisticated designs. Using the Globally Asynchronous Locally Synchronous (GALS) design approach potentially jeopardize this. Asynchronous handshaking, as the name suggests, will be used. The biggest source of power usage is addressed by removing the world clock. Additionally, synchronous blocks work asynchronously with regard to one another, and each synchronous clock's operating frequency can be changed in accordance with its requirements, lowering the average frequency and lowering overall power consumption.

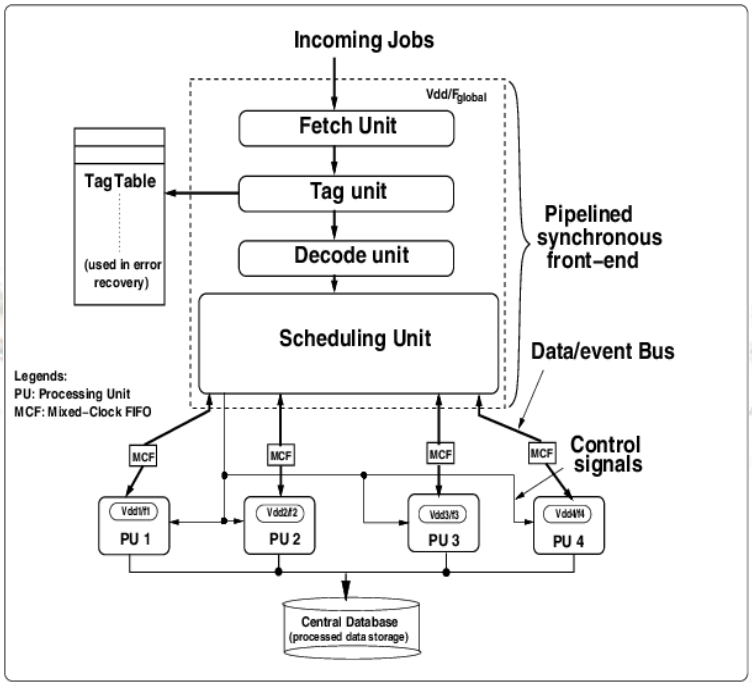

Fig: Proposed GALS system architecture

(1)GALS methodology

The synchronous design style is slightly influenced by the GALS design approach. The division of the synchronous system into smaller synchronous blocks and the establishment of asynchronous communication between the synchronous blocks are two ways in which the GALS design expands the synchronous design methodology.

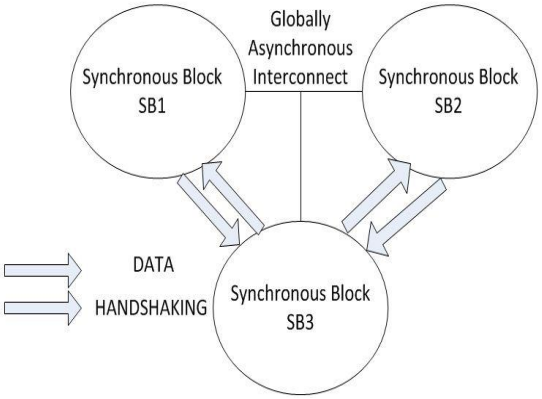

Fig: GALS methodology

III.ASYNCHRONOUS DISPLAY CONTROLLER

The majority of digital circuits being developed nowadays are synchronous. All synchronous designs presumptively use a single, widely dispersed time signal. This presumption fails to take into account issues like dangers and the changing state of the circuit. It is anticipated that a system created without this presumption will deliver superior outcomes. This ubiquitous and discrete time assumption is removed by asynchronous design, which has a number of advantages such as low power consumption and the avoidance of timing problems on a global scale [17]. Even though synchronous designs are now quite ubiquitous and widely used, asynchronous design is always necessary. One synchronous system can talk to another using asynchronous logic. The asynchronous design logic was made simpler with the development of several approaches. The Globally Asynchronous Locally Synchronous (GALS) design is one such approach.

(1)Design of asynchronous display controller

By dividing the synchronous display controller presented in the previous chapter into distinct synchronous blocks, the asynchronous display controller was created utilizing the GALS methodology. Similar to the synchronous display controller, the asynchronous version uses registers to identify boundaries like the show end and the blanking period and counters to maintain track of the dot pattern supplied consecutively into the display.

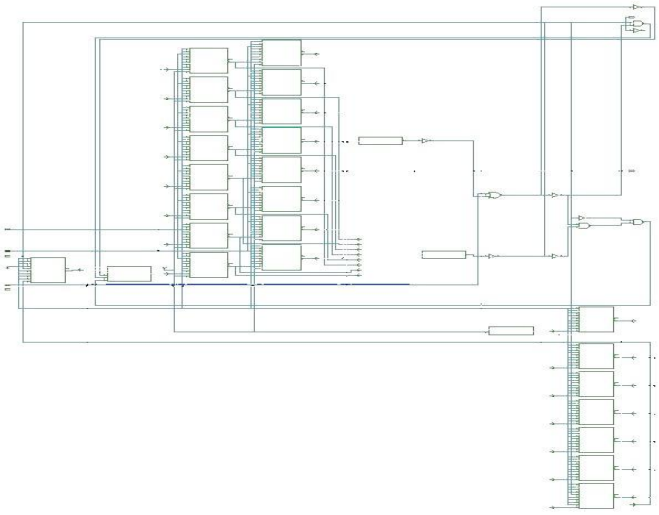

Figure . Schematic of the asynchronous counter

1) The Flip-Flop
2) The Incrementer
3) The Comparator

The flip-flop is designed to operate when the previous module generates a completion signal, whereas the comparator is designed to operate at the clock edge. The incrementer is made to operate in an asynchronous fashion. The handshake mechanism of communication links the three blocks. To ensure that the constituent blocks operate sequentially without competing with one another, a number of intermediate completion signals are generated.

(2)Power Analysis of Synchronous and Asynchronous Designs

the need for low power design is motivated by several factors, such as the emergence of portable systems, thermal considerations, reliability issues, and finally environmental concerns. Thus, an in-depth power analysis is required to design a low power system and avoid these problems.

Power Analysis in Synchronous Display Controller

Dynamic switching power consumption, or Psw, is the main cause of power consumption in digital circuits. The frequency and voltage levels for a specific design are fixed by equation (1.2). The capacitance is determined as the product of the load capacitance of the circuit and all parasitic capacitances from all interconnects in the circuits. The average number of switching transitions per clock cycle, denoted by the activity factor N in equation (1.2), is the sole variable that has to be determined. The VCD file, which was created by simulating the RTL design for a predetermined number of clock cycles, can be used to observe the number of signal switching transitions. With the 39 clock running at a frequency of 500 MHz, the synchronous display controller was simulated for roughly 10,000 clock cycles. It was discovered that the design had about 3, 81,019 switching occurrences. The total parasitic capacitance of the circuit was estimated to be 1ff for convenience of calculation, and the circuit was run at a global operating voltage of 2.5 V. Now, the synchronous display controller's dynamic switching power may be computed as follows:

$$Psw = 1/2\ Co\ Vin^2\ N\ f = 1/2*10^{-15}*(2.5)^2 * 38 * 500 * 10^6 = 59.375\ \mu W$$

The circuit's signal transitions, as computed, account for the majority of this dynamic power. This power rises as the clock frequency rises since the circuit will experience more transitions.

(3)Power Analysis in Asynchronous Display Controller

The dynamic power consumption in the asynchronous display controller was also calculated using equation . As in the synchronous one, the global operating voltage was 2.5 V, and the total parasitic capacitance was assumed to be 1 ff for ease of calculation. The number of signal switching transitions was observed from the VCD file. The asynchronous display controller was simulated for about 10,000 clock cycles with the clock running at a frequency of 100 MHz; the design had about 3, 52,472 switching events. Now the dynamic switching power in the synchronous display controller can be calculated as below:

$$Psw = .\ 1/2Co\ Vin^2\ N\ f$$
$$= .\ 1/2 * 10^{-15} * (2.5)2 * 35 * 100 * 10^6$$
$$= 10.938\ \mu W$$

The dynamic power thus obtained was observed to be much less than the one obtained for the synchronous display controller. This power reduction is mainly due to the reduced dependency on the clock signal in the asynchronous display controller. In addition, in the asynchronous display controller, the clock ran at 100 MHz, and the energy required to drive the clock was much less than the synchronous one.

IV. CONCLUSIONS

This paper offers a fresh method for utilising asynchronous logic in low power designs. The development of portable devices and their applications has greatly increased the necessity of low power design. other elements, including Even in the early stages of design, designers are compelled to explore for power reduction methods due to thermal, reliability, and environmental issues. The clock signal and clock distribution network in synchronous circuits use around 50% of the total chip power [25]. The dynamic capacitive switching power in digital systems is the main energy guzzler. In high-speed circuits, the capacitive switching power increases according to the clock frequency.

V. REFERENCES

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