A LOW POWER TIMING ERROR TOLERANT SYSTEM

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Abstract: ***This paper's major objective is to create a timing error-tolerant circuit that can identify and repair timing problems, which are currently receiving more attention due to the high rate at which they occur in semiconductor circuits.The timing margin between following clocks may be in danger from even a small external disruption. These timing issues can be solved in a number of ways, but they are all too challenging to apply. This study provides a cutting-edge method for quickly correcting timing errors that is tolerant of timing errors and uses a simple methodology. The proposed system, which fixes a timing error by changing a clock in a flip-flop, can do so without losing time, unlike the clock-based method.***

Key Words: Master clock generator, Time borrowing circuit, Transition detector, and Timing Error.

1.INTRODUCTION

Timing errors are an increasing reliability concern in nanometer technology, high complexity, and multivoltage\frequency integrated circuits. Process variability in device and circuit parameters is one of the primary challenges currently faced by the semiconductor industry. Besides static variations that occur during chip fabrication, dynamic parameter variation,resulting from environmental and workload changes is also possible during the chip's operation. The timing error occurs because of the delay in combinational circuits that are located between the memory elements. After the edge of the clock, the delayed data cannot be stored in the memory element properly. To deal with the timing error, many related methods have been proposed.

In order to increase tolerance to delay variations in logic stages in a pipelined system with a minimal performance penalty (less than a clock cycle), this study offers a technique to anticipate timing issues while operating the system at a clock period less than the critical path delay. Time-borrowing techniques have been introduced to get around the clock's penalty. The entire system is not delayed in recovering from a timing error since it borrows time from the following pipeline stage to repair a timing error. To fix a timing problem, it has two master latches and one slave latch.

2.EXISTING SYSTEM

The "pulsed latch" technology is used in today's error tolerant systems. The timing constraint is relaxed by a pulsed latch's time borrowing capabilities. The pulsed latch can sample the proper data due to it's time borrowing behavior until the path delay is smaller than the total of the clock period and time borrowing window. Once again the borrowed time is added to the next stage path delay. Inturn, which makes path delay larger than the total of the clock period and time borrowing window. So pulsed latch in this stage will be unable to sample the data properly. Here the errors in each stage got increased.

In this technology, the whole system was controlled by a single clock including the error correcting system.As a result, when the pulsing latch borrows the clock, the clock of the entire system changes, creating an abrupt behavior for a brief amount of time, resulting in increased power consumption for a brief period.

Drawbacks:

- High power consumption
- Can't correct and detect the errors at a time
- Additional clock is required for error recovery

3.PROPOSED SYSTEM

As the clock frequency rises, the timing-error rate also rises. Critical paths in the circuit are prone to timing problems because the clock period is getting smaller.. Modern integrated circuits perform poorly due to temperature, power supply, and CMOS process changes, which contributes to the frequent occurrence of timing mistakes. The delay of the circuit can significantly vary between the best and worst process, voltage, and temperature (PVT) conditions when the supply voltage falls.. With the 0.4-V operation, the logical path with the worst case is 12x slower than that with the typical case Additionally, timing The threshold voltage is lowered as a result of CMOS's negative-bias temperature instability (NBTI), which in turn lengthens logic paths. In order to construct dependable systems, a timing-error-tolerant approach is crucial. The combinational circuits positioned between the memory components' timing elements have a delay, which causes the timing mistake. The delayed data cannot be correctly stored in the memory element once the clock has reached its edge.

faults are greatly influenced by transistor ageing problems. Numerous related solutions have been put up to address the timing problem.The temporary error-detection system is just one example of a timing-error-tolerant system.

It identifies the transient timing fault that is propagated from the input with little hardware overhead by comparing the flip-flop's output with a delayed output. However, it is unable to rectify the issue; it can only notice it with a delayed time. Other solutions for the identification and rectification of timing errors in the design of microprocessors have been presented based on the prior system using the delayed methodology.With an XOR gate, they contrast the input and output of a flip-flop. XOR gates and memory components are used to adjust the output when a defect signal is detected. Following the sacrifice of one clock for the recovery, they resume normal operation because the time interval is necessary for mistake detection and correction.

Time-borrowing techniques have been developed to get around the clock's penalty. The entire system is not delayed for the recovery of a timing error since it corrects a timing error by borrowing time from the following pipeline level. To fix a timing issue, it comprises of two master latches and one slave latch. While the borrowing time can prevent system delays, the system still needs too many complicated mechanisms and circuits. Another current system that corrects a timing problem by borrowing time has been demonstrated, and it, too, does so without the need for a separate clock. It has a timing violation predictor that can find timing issues halfway along the critical path.

After an error is detected, the system controls the flip-flop to become a transparent state. While the system can avoid the penalty of the clock, it requires a large amount of hardware, such as an additional flip-flop and latch. Furthermore, since the location of the halfway of the combinational circuits is inaccurate and it is hard to be chosen, the transparent window can be made erroneously. In this article, we propose a timing-error-tolerant method that can correct a timing error immediately through a simple mechanism. In the critical path, the abnormal data transition after the rising edge of the clock, which is caused by a timing error, is detected and corrected by controlling the transparent window of the clock.

A minimal amount of logics directly corrects the timing problem. In addition, we introduce our time-borrowing approach that handles successive mistakes. The adjusted CLK in the second stage keeps a transparent window open for long enough to allow regular data to be saved without modifying the system CLK if the timing error happens in two stages consecutively. In comparison to the current timing-error mitigation solutions, the entire circuit has a smaller hardware overhead and performs better overall due to its compact circuit topology. Analogue and digital simulations were used to research the suggested system.

The proposed circuit was specifically thoroughly simulated with CMOS circuit architecture to handle PVT fluctuations. A microprocessor was used as one of the benchmarks when the suggested technique was put into practise. Comparisons with other traditional methods were also made with regard to hardware overhead and performance. It was confirmed that, when compared to the present system, the suggested system performs better while using less hardware.

4.BLOCK DIAGRAM OF PROPOSED TIMING ERROR TOLERANT SYSTEM

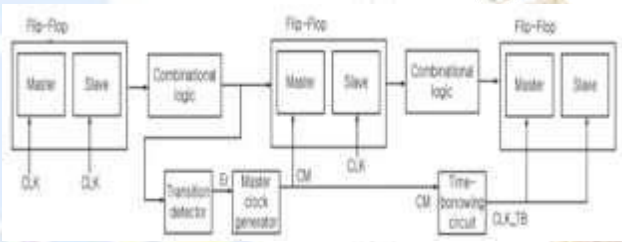

Fig1.Block diagram of timing error tolerant system

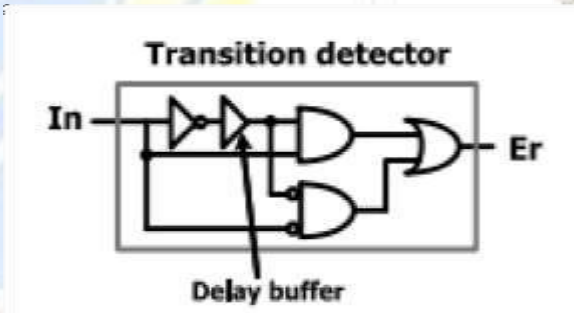

Fig1(a) Internal circuit of Transition Detector

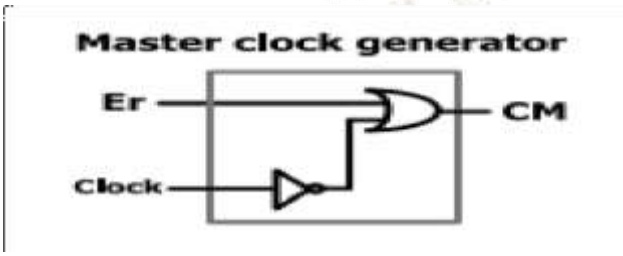

Fig1(b) Internal circuit of master clock generator

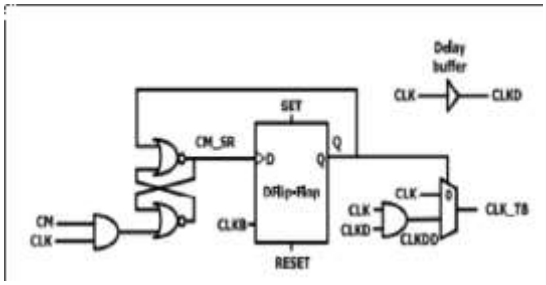

Fig1(c) Internal circuit of time borrowing circuit

5. WORKING OF PROPOSED TIMING ERROR TOLERANT SYSTEM

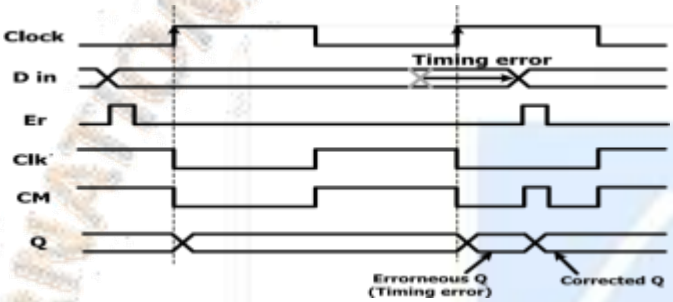

Fig2.Operation of the proposed system when a timing error occurs

A novel system that is capable of correcting a timing issue has been created. The suggested system may identify a delayed input of the flip-flop, and the flip-flop passes through the data by creating a transparent window when a timing mistake delays an input's arrival on the flip-flop. A "transition detector" and a "master clock generator" make up the proposed system, as shown in Fig. 1(a). When a flip- flop's input transition is detected, the "transition detector" generates a pulse of the signal that indicates an error. The "master clock generator" only generates a pulse for a specific duration when a clock is high, based on the output of the transition detector.. Since a pulse controls the flip-flop's master clock while it is "1," it creates a transparent window and transfers input to output while it is in this state. As a result, the flip-flop's anomalous data can be recovered using normal data that has been delayed. A pulse is created with a minimum time that is necessary for the setup time in order to prevent hold time violation. The recovery procedure from a timing issue in the suggested system is fully addressed, as seen in Fig. 2. The flipflop 2 stores aberrant data to the output Q as a result of the delayed input data when a timing fault affects the input data.

The transition detector, which is situated between a combinational circuit and the flip-flop 2, emits an error pulse after the delayed normal data have arrived on the input of flip-flop 2. Using an inverter and an AND gate, the transition detector can recognise both a rising and a falling edge in the data. Additionally, the transition detector uses a delay buffer to generate a pulse with a customised period that sustains the transparent window for a sufficient amount of time. Based on the error pulse and clock, the master clock generator creates the master (CM) clock.

The OR gate and inverter in the master clock generator cause a CM to stay high after a timing error for a defined period of time. Flip-flop 2 becomes transparent when the CM is high and stores the delayed normal input through it. As a result, the incorrect output Q is corrected using the right input. The suggested system detects and corrects the timing mistake while the clock is high since the timing error typically happens after a rising edge of the clock. The suggested approach is used for critical pathways when the combinational circuit's latency exceeds the clock period's half-life.

6. ADVANTAGES

The benefits of this particular System are as follows:

- The controlling function of the clock signal eliminates the requirement for an additional clock for error recovery.
- Instantaneous error detection and correction.
- Low Area overhead because there are fewer logic involved.
- Avoiding the time-borrower circuit's clock penalty.

7. FUTURE SCOPE

Every component, such as memory and communication devices, has shift registers in greater quantity. This paper demonstrates how a 264 bit shifter using pulsed latches may be extremely power-efficient.. Shift registers will likely be used or implemented for very high-speed and high-bit-rate devices in the future, which will make them portable and widely applicable.

8. RESULTS

Schematic diagram of proposed system and waveforms were observed as follows:

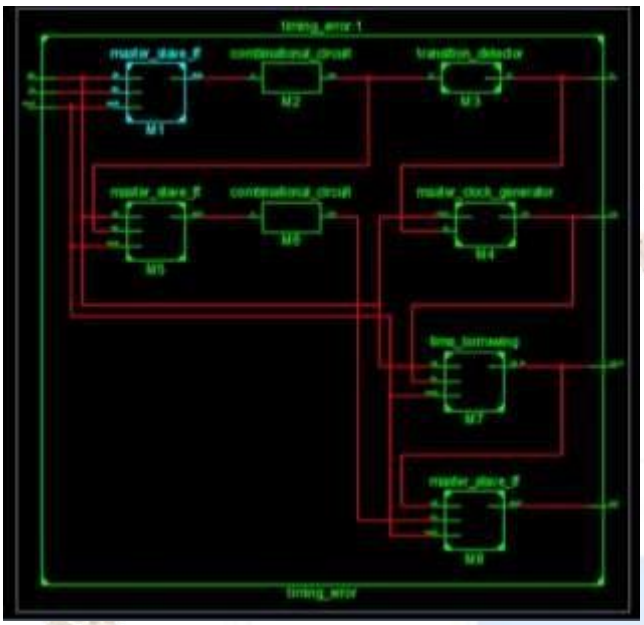

Fig3.Schematic Circuit of Proposed system using Time Borrowing Technique.

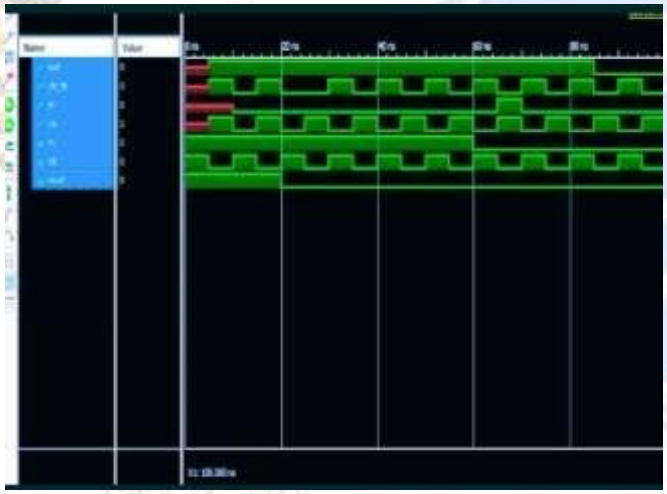

Fig4.Wave forms

9. CONCLUSION

With the help of the time borrowing technique, we can demonstrate a practical way to identify and rectify timing faults in timing error-tolerant circuits. Controlling the clock's transparent window allows the critical path to identify and repair anomalous data transitions that occur after the clock's edge.

Through a minimal amount of logic, the timing error is directly repaired. In addition, our method for borrowing time that addresses the successive-stage mistake is presented. Timing errors can be tolerated if they happen repeatedly in the second stage thanks to modified CLK, which keeps the transparent window open for long enough.

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