A Low Power High Speed Sense Amplifier Based Flip Flop in 45nm MTCMOS

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Abstract - A sense-amplifier-based flip-flop (SAFF) suitable for low-power high-speed operation. With the employment of a new sense-amplifier stage as well as a new single-ended latch stage, the power and delay of the flip-flop is greatly reduced. The proposed SAFF can provide low voltage operation by adopting MTCMOS optimization. The proposed SAFF delay and the power are smaller than those of the existing master-slave flip-flop (MSFF).The power-delay-product of the proposed SAFF improves compared with the conventional SAFF and MSFF, respectively the area of the proposed flip-flop decrease, the proposed SAFF could provide robust operation even low power supply voltages. But in this design we are using 45nm technology by using this technology we can get the required output by giving 1LVT (low threshold voltage).

Index Terms - Low power,high speed, flip-flops,sense amplifier,MTCMOS

I. INTRODUCTION:

Amplifier is the generic term used to describe a circuit which produces and increased version of its input signal. However, not all amplifier circuits are the same as they are classified according to their circuit configurations and modes of operation. In "Electronics", small signal amplifiers are commonly used devices as they have the ability to amplify a relatively small input signal, for example from a *Sensor* such as a photo-device, into a much larger output signal to drive a relay, lamp or loudspeaker for example. There are many forms of electronic circuits classed as amplifiers, from Operational Amplifiers and Small Signal Amplifiers up to Large Signal and Power Amplifiers. The classification of an amplifier depends upon the size of the signal, large or small, its physical configuration and how it processes the input signal that is the relationship between input signal and current flowing in the load.Amplifiers can be thought of as a simple box or block containing the amplifying device, such as a Bipolar Transistor, Field Effect Transistor or Operational Amplifier, which has two input terminals and two output terminals (ground being common) with the output signal being much greater than that of the input signal as it has been "Amplified". An ideal signal amplifier will have three main properties: Input Resistance or (R_{IN}), Output Resistance or (R_{OUT}) and of course amplification known commonly as Gain or (A). No matter how complicated an amplifier circuit is, a general amplifier model can still be used to show the relationship of these three properties.The amplified difference between the input and output signals is known as the Gain of the amplifier. Gain is basically a measure of how much an amplifier "amplifies" the input signal. For example, if we have an input signal of 1 volt and an output of 50 volts, then the gain of the amplifier would be "50". In other words, the input signal has been increased by a factor of 50. This increase is called **Gain**.Amplifier gain is simply the ratio of the output divided-by the input. Gain has no units as it's a ratio, but in Electronics it is commonly given the symbol "A", for Amplification. Then the gain of an amplifier is simply calculated as the "output signal divided by the input signal".

II. LITERATURE SURVEY

[1] Jeong, H.; Oh, T.W.; Song, S.C.; Jung, S.-O. Sense-amplifier-based flip-flop with transition completion detection for low-voltage operation. 2018.A high-speed and highly reliable sense amplifier-based flip-flop with transition completion detection (SAFF-TCD) is low supply voltage (VDD) operation. The SAFF-TCD adopts the internally generated detection signal to indicate the completion of sense-amplifier stage transition. The detection signal gates the pull-down path of the sense-amplifier stage and the slave latch, thus overcoming the operational yield degradation, current contention, and glitches of previous SAFFs.

[2] Jeong, H.; Park, J.; Song, S.C.; Jung, S.-O. Self-Timed Pulsed Latch for Low-Voltage Operation With Reduced Hold Time. IEEE J. Solid-state Circuits 2019.A self-timed pulsed latch (STPL) is proposed for low VDD operation. By comparing input and output, the transparency window is adaptively generated in STPL, which resolves the hold time problem of the conventional pulsed latch.

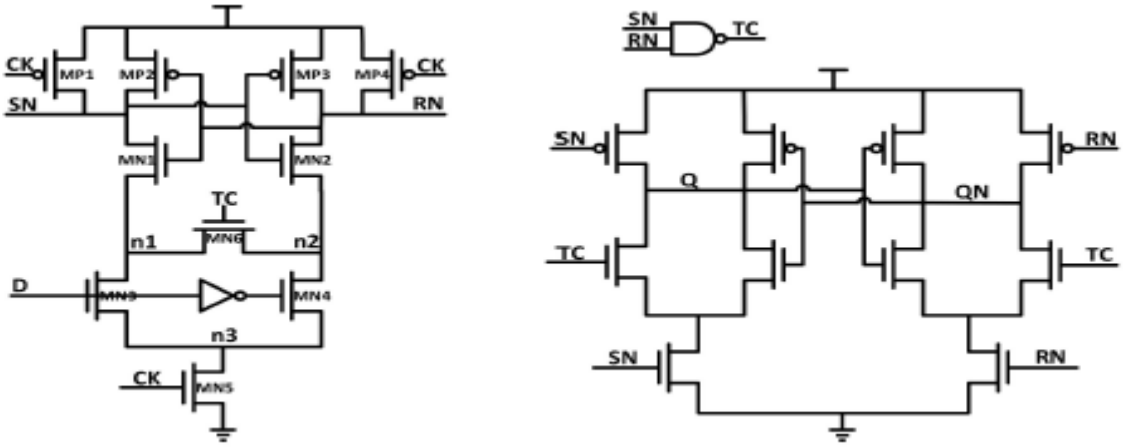


Figure 1:Schematic of the latche of jeong's SAFF

[3] Kim, J.-C.; Jang, Y.-C.; Park, H.-J. CMOS sense amplifier-based flip-flop with two N-C2MOS output latches. Electron. Lett. 2000, 36, 498–500.Nikolic's flip-flop was proposed to further increase the operating speed. NAND SR latch of [1] was replaced by a combined circuit of a cross-coupled inverter latch and two inverting buffers. However, the power consumption of the flip-flop is much larger than that of the conventional SAFF. In the new SAFF proposed in this work, the NAND SR latch in was replaced by two NC2 MOS latches. The new SAFF gave the fastest operating speed from among the flip-flops compared in this work, while the power consumption increased moderately compared to that of the conventional SAFF

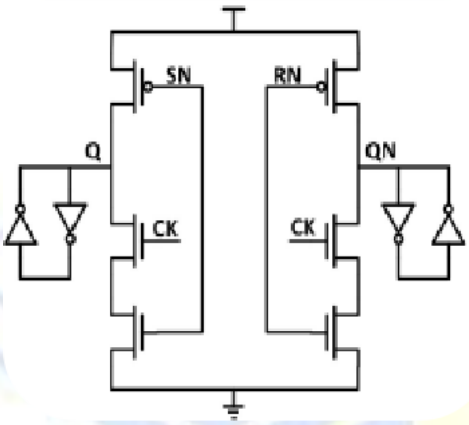


Figure 2:Schematic of the latche of Kim's SAFF

[4] Strollo, G.M.; De Caro, D.; Napoli, E.; Petra,N.Anovel high-speed sense-amplifier based flip-flop. IEEE Trans.2005.A new sense-amplifier-based flip-flop is presented. The output latch of the proposed circuit can be considered as a hybrid solution between the standard NAND-based set/reset latch and the NC-2MOS approach. The proposed flip-flop provides ratio less design, reduced short-circuit power dissipation, and glitch-free operation. The simulation results, obtained for a 0.25- m technology, show improvements in the clock-to-output delay and the power dissipation with respect to the recently proposed high-speed flip-flops.

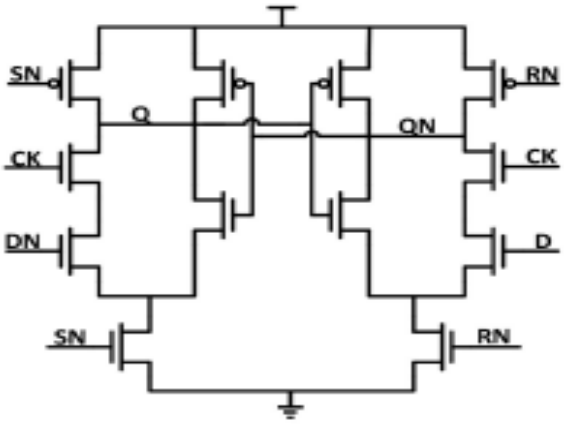
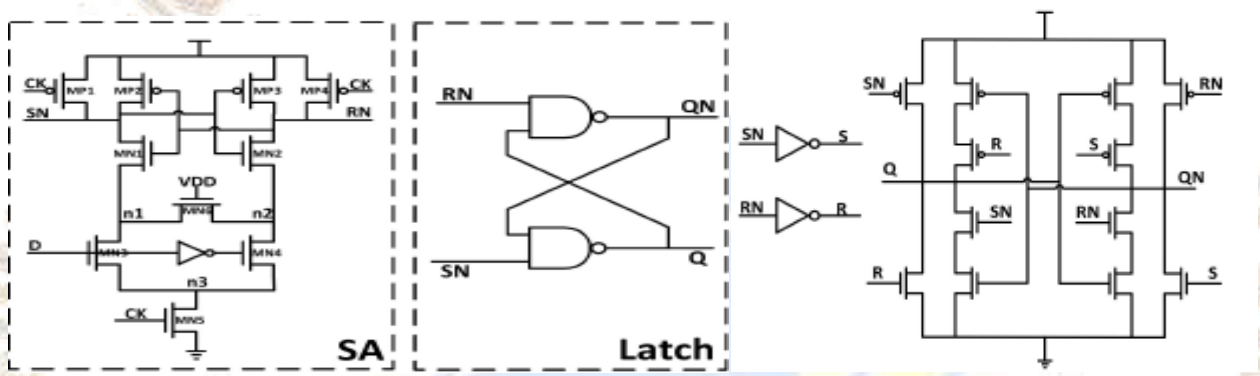


Figure 3:Schematic of the latche of strollo's SAFF

[5] Matsui, M.; Hara, H.; Uetani, Y.; Kim, L.; Nagamatsu, T.; Watanabe, Y.; Chiba, A.; Matsuda, K.;Sakurai, Solid-State Circuits 1994.The fast speed and small area are achieved by a novel sense-amplifying pipeline flip-flop (SAFN) circuit technique in combination with tt MOS differential logic. The SA-FN, a class of delay flip-flops, can be used as a differential synchronous sense-amplifier, and can amplify dual rail inputs with swings lower than 100 Mv.

III. EXISTING MODEL

The schematic of the conventional SAFF, which is composed of a SA and a NAND2-based set reset (S-R) latch, is shown in Figure 2a. The SAFF operates as follows. The voltage of SN and RN is pre-charged to VDD while the CK is low; the output data are maintained by the latch. At the rising edge of CK, the pre-charge transistors MP1 and MP4 are turned off and MN5 is turned on. One of the pre-charge nodes (SN and RN) is discharged to 0 while the other remains VDD, depending on the input data. Then, the latch captures the new data from the SA stage. The always-on transistor MN6 is used to maintain the output of the SA when CK is high. For example, SN is discharged to 0 in response to D = 1 at the rising edge of CK, and SN needs to be maintained at 0 during the positive half cycle of CK. D may change to 0 during the positive half cycle, thus another path to 0 should be provided to SN, and MN6 works at this time. The main trouble with the conventional SAFF is the unbalanced delay of the S-R latch as well as the large power of the pre-charge operation. Moreover, the always-on transistor decreases the robustness of the SAFF at low supply voltages



(a) **(b)**

Figure 4. (**a**) Schematic of the conventional sense-amplifier-based flip-flop (SAFF); (**b**) Schematic of the latch in Nikolic's SAFF

Nikolic et al. proposed a latch for the SAFF, which was composed of two inverters and several complex logics to eliminate the delay dependence between Q and QN in the conventional SAFF, so as to decrease the delay of the SAFF. The schematic of the latch is shown in Figure 2b. The two inverters are applied to get the inversion of SN and RN, and the output Q and QN is directly generated by the four signal SN, RN, S and R. The dependence between Q and QN is removed and the CK-to-Q delay is decreased. Since the delay of the inverters and complex logic cannot be ignored, the optimization of the delay in this way may not meet the expectations.

IV. PROPOSED MODEL

The schematic of the proposed SAFF is shown in Figure 5. As shown in Figure 5, the SAFF is composed of a SA stage and a slave latch, similar to the previous SAFFs. As described in previous sections, the SA stage could capture the data right after the rising edge of CK and the slave latch is applied to maintain the output during the negative half cycle of CK

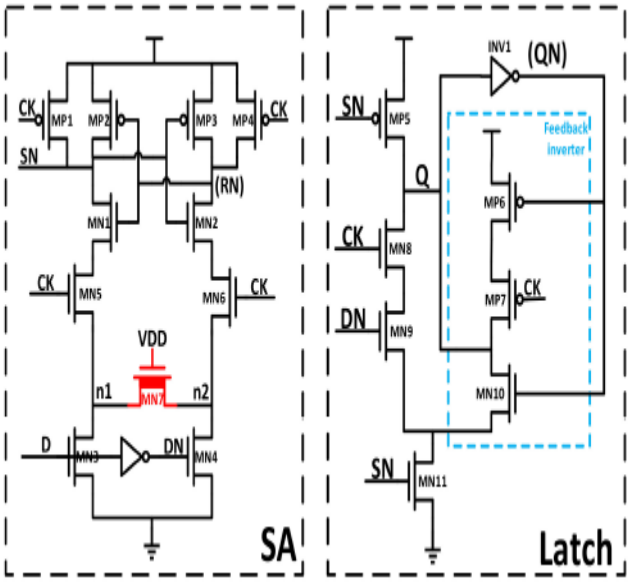


Figure 5. Schematic of the proposed SAFF.

The SA stage in the conventional SAFF needs to charge all the internal nodes during pre-charge operation, and some of the nodes such as n1, n2 and n3 in Figure 2a are discharged to VSS during the data-capturing operation no matter what the input data are. Actually, the pre-charge operation of n1, n2 and n3 has no practical effect on the function of the SA and is a waste of power. The voltages of n1, n2, and n3 are charged close to the power supply voltage during pre-charge operation, and the sizes of the transistors MN3 and MN4 are large to decrease the propagation delay, so the pre-charge operation of these nodes is a large waste of power consumption. In this paper, the structure of the SA is changed; the NMOS controlled by CK (MN5 in Figure 2) is split into two (MN5 and MN6 in Figure 5) and moved to connect directly to the back-to-back inverter, as shown in Figure 5. Through the conversion, the nodes related to MN3 and MN4 no longer need to charge during pre-charge operation since the transistors MN5 and MN6 are o_ when CK is low. The voltages of n1 and n2 in Figure 5 remain low throughout the operation. Thus, the power. Of the pre-charge operation is greatly reduced. Since pre-charge power is an important part of the power consumption of the SAFF, the power consumption of the proposed SAFF can be greatly reduced.The proposed SA structure can also improve the hold time of the proposed SAFF. The new SA stage can capture the input data faster at the rising edge of CK. This is mainly because the internal nodes n1 and n2 remain low during the operation, and the discharge time of the internal nodes is reduced. Thus, the hold time of the proposed SAFF is reduced. Even though faster data capture increases the setup time of the proposed SAFF, the increase is very small because the discharge time of the internal nodes is short.`A new single-ended latch is applied to the proposed SAFF. The proposed latch combines the advantages of Strollo's latch and Lin's latch to achieve fast and energy efficient operation. The first stage of the latch shown in Figure 5 is similar to that of Strollo's latch to achieve glitch-free operation. The glitch of Lin's latch is perfectly removed. This is mainly due to the insertion of MN9. When D is high, DN is low and the pull down path is totally cut o_ by MN9. Thus, the glitch is removed. The back-to-back inverters used for data storage are modified to overcome the current contention. For the output Q's transition from low to high, which means the voltage of SN is low, the feedback inverter is cut o_ by MN11. Similarly, for the output Q's transition from high to low, the feedback inverter is cut o_ by MP7. As a result, the effect of the feedback inverter on the output transition is completely eliminated. Since the latch has nothing to do with RN, the sizes of the transistors related to RN generation in the SA stage could be reduced to reduce power consumption. The 1_ inverter INV1 in the latch could provide complementary output QN when necessary, and the delay difference between Q and QN is the same as MSFF, an inverter delay.As described the always-on transistor leads to function failures at low supply voltages. Even though the detection logic solves the low voltage function failures well, the complex logic increases the delay and power consumption. In this paper, MTCMOS optimization is employed to overcome the problem. To avoid suffering low voltage function failures, the driving capability of the always-on transistor should be weaker than that of the pull-down transistors. When the driving capacity of two stacked LVT-NMOSs and the always-on transistor becomes larger than that of two stacked LVT-NMOSs due to technological variation, the SAFF suffers function failures. When the always-on transistor is LVT-NMOS, three LVT-NMOSs are stacked. The current of three stacked LVT-NMOSs can be larger than that of two

stacked LVT-NMOSs (I1 / I2 < 1) at low supply voltages, and function failures occur. When the always-on transistor is changed to HVT-NMOS, which means two LVT-NMOSs and one HVT-NMOS are stacked, the function failures no longer occur since the current of two stacked LVT-NMOSs and one HVT-NMOS is always smaller than that of two stacked LVT-NMOSs (I1 / I3 > 1 all the time). Furthermore, the current of two stacked LVT-NMOSs and the always-on transistor needs to be larger than the leakage current to ensure correct operation. When the always-on transistor adopts HVT-NMOS, the condition is still satisfied. Therefore, the problem of low voltage function failures can be well solved by multi-threshold optimization. In the proposed design, the always-on transistor is high-threshold, while others are low-threshold, as shown in Figure 5.

V. RESULTS

The proposed SAFF has been designed based on **45** nm technology. In order to verify the validity of the proposed SAFF, the MSFF, the conventional SAFF, Nikolic's SAFF, Lin's SAFF and Jeong's SAFF have also been designed based on the same technology for comparison. With the same settings is adopted to perform all post-layout simulations for comparisons. The performance comparisons such as of the area, power consumption, CK-to-Q delay, setup time and hold time of the various flip-flops are described in detail below table.

Power and delay comparison of Existing and Proposed SAFF

Type of SAFF	Power(mw)	Delay(ns)	Area of MOSFETS
Nikolic's SAFF	7.3	30	28
Strollo's SAFF	1.2	30	24
Jeong's SAFF	1.9	40	26
Lin's SAFF	2.4	0.3	20
Proposed SAFF	0.04	0.4	22

Comparision Table 1:

Designs, waveforms and output screenshots:

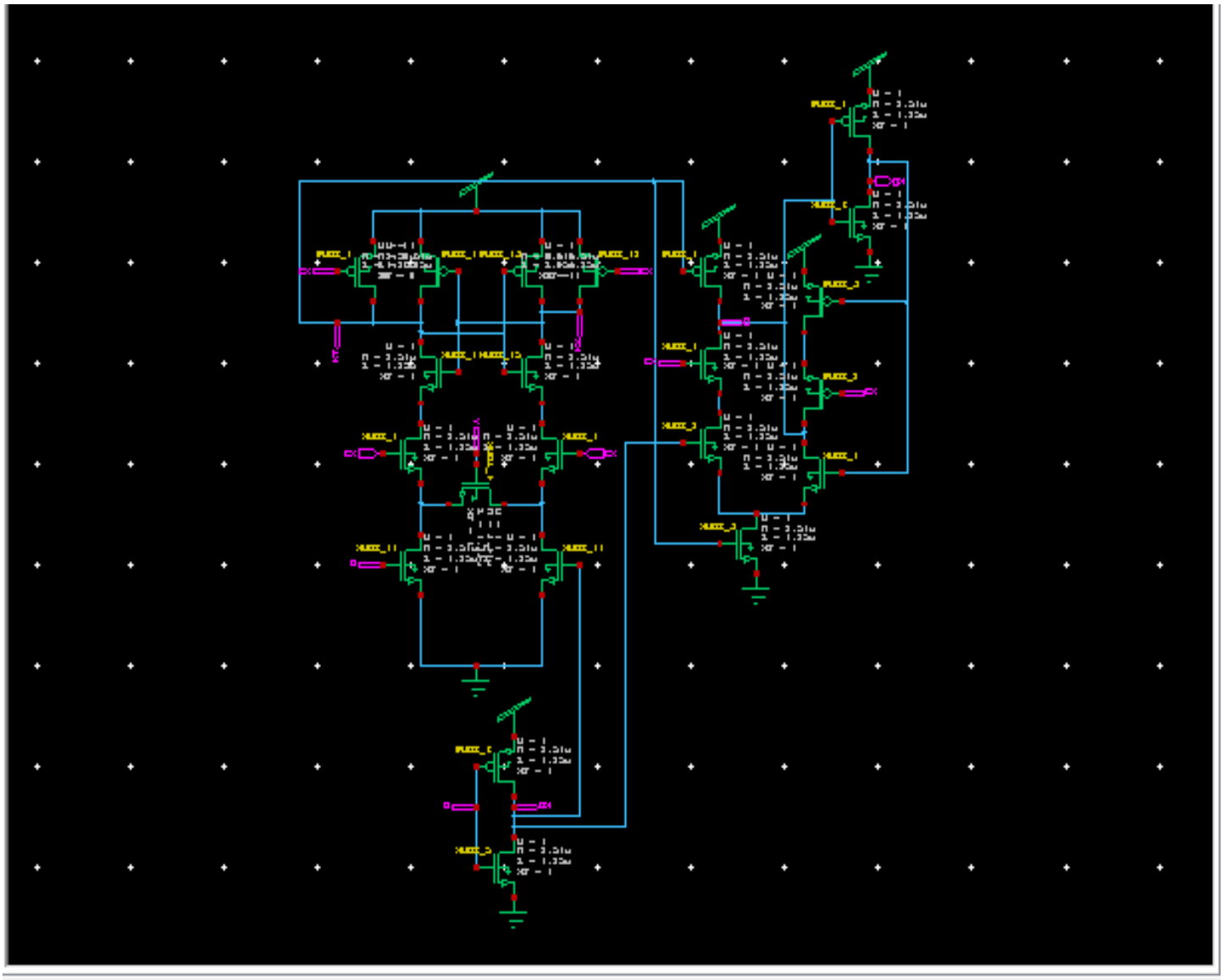


Figure 6: Schematic of the proposed SAFF is shown in the figure

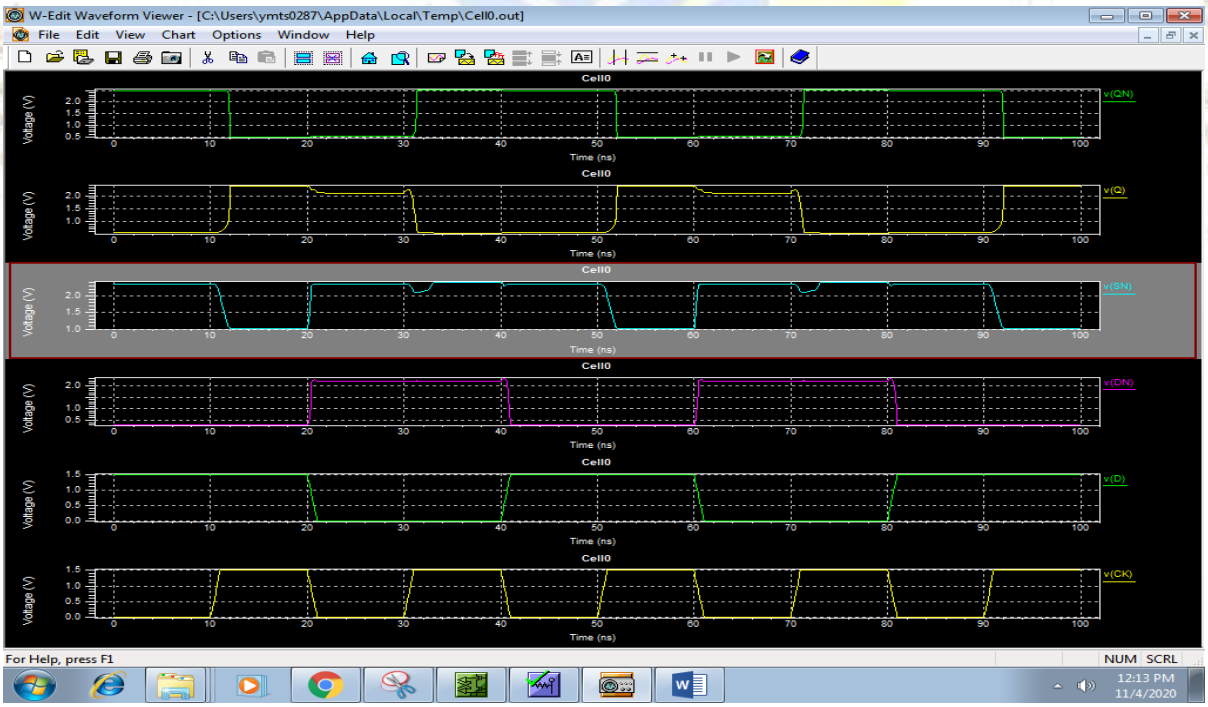


Figure 7: Wave forms for proposed SAFF

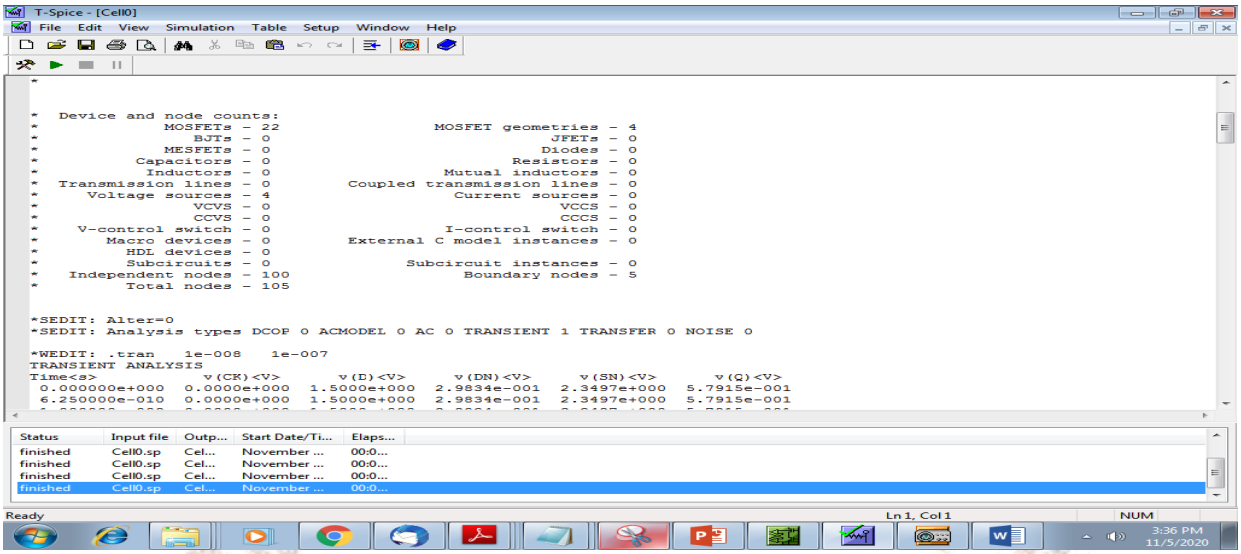


Figure 8: Area of the proposed SAFF Power of the proposed SAFF

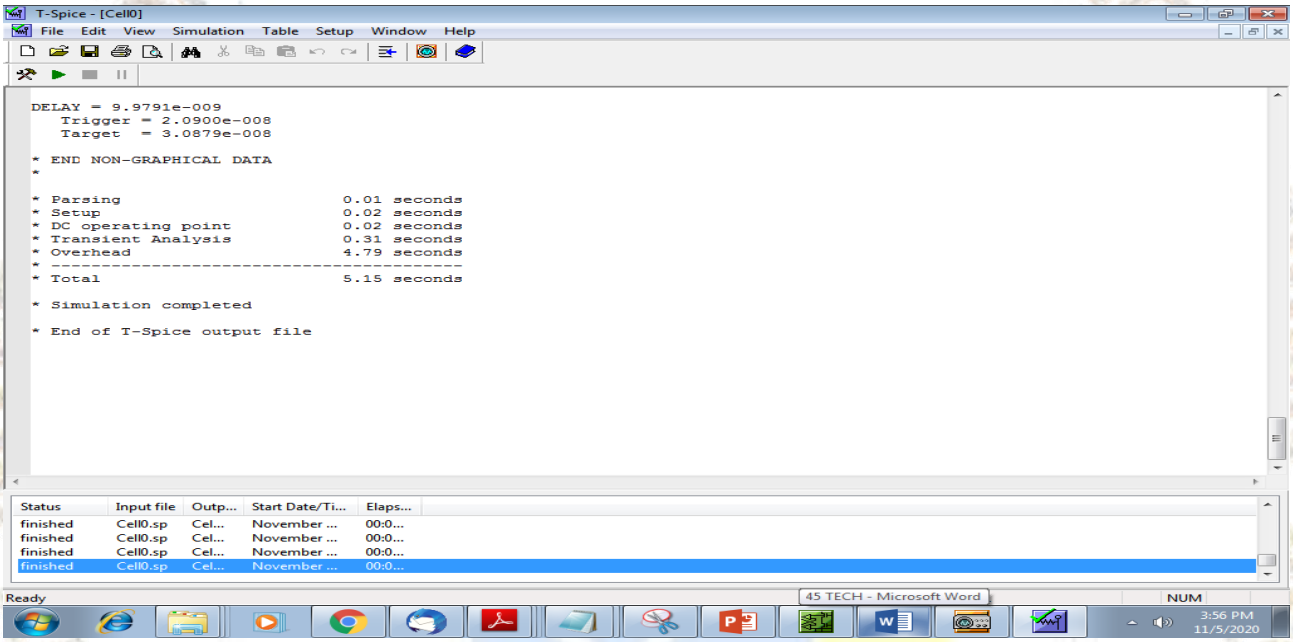


Figure 9: Delay of the SAFF

VI. CONCLUSION

A low-power high-speed SAFF is proposed in this paper. By using 45nm technology structure of the SA stage is proposed to minimize the pre-charge power of the SAFF. Additionally, a glitch-free and contention-free single-ended latch is proposed. With the employment of the new SA stage and the single-ended latch, the delay and power of the SAFF are greatly optimized. The power-delay-product of the proposed improvement compared with that of the conventional SAFF.The improvement is when compared with the MSFF, which indicates that the proposed SAFF is a good choice for replacing MSFFs in digital systems to provide low-power, high-speed operation.

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