Effectual Adder Using GDI Technique

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ABSTRACT

In this paper we present an effective adder using the GDI technique, which is mostly used in modern digital electronic devices. In order to achieve high performance in terms of Area, Power consumption and Delay, the performance of the full adder can be greatly improved by using GDI technique. The proposed Full adder is simulated with the Cadence tool and virtuoso platform.

Index terms: GDI technique, Full Adder, Area, Power consumption, Delay.

I.INTRODUCTION

Large scale integration growth has enhanced the electronic industry, and the impact of VLSI in it is inevitable. VLSI technology integrates complex components on a single chip. An analog circuit technique demands a digital domain to save power. The realization of a low power, low area circuit is very important due to the demand for electronic devices like mobile phones, laptops and tablets. In order to increase the throughput of adder we are using GDI technique in this paper.

In general, the performance of full adders in terms of delay, power consumption, area and high speed can be influenced by the GDI technique. AND, OR, XOR logic gates are used to implement the full adder logic style. The GDI technique is used because it has the advantage of low power consumption and reduces the count of transistors with low complexity when compared to the other techniques..

II. EXISTING METHOD

Various papers have been published related to Full adder using CMOS technology for Energy efficient Arithmetic applications. To implement CMOS full adders, different logic styles were used. They are DPL (Double pass transistor Logic), PTL (Pass transistor logic), and SRCPL (Swing Restored Complementary pass transistor Logic). These logical styles are too complex in nature to implement a full algorithm. So, to implement a CMOS full adder 54 transistors are required.

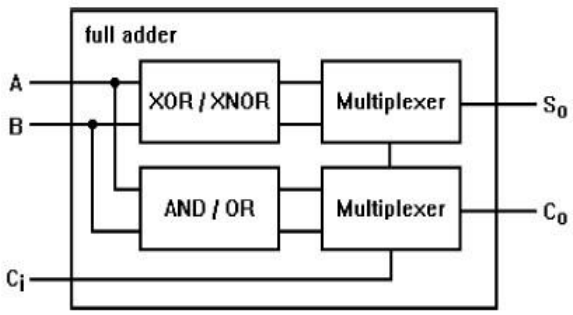

Fig .1: Logic scheme for Energy Efficient Full Adder

The above figure represents the Full adder Block diagram. A, B, Ci are inputs and S0,C0 are outputs. Now the operation of Full adder is when Ci=0, S0=A XOR B, and C0 = A AND B. When Carry input (Ci=0), the XOR, AND gates becomes active. The Full adder

performs the operation & produces Sum(S0) and Carry (C0) as an output. When Ci=1, S0 = A XNOR B, and C0 = A OR B, When the Carry input (Ci=1) is set to 1, the XNOR and OR gates become active. The full adder performs the operation and produces the output as sum (S0) and carry(C0).

III. PROPOSED TECHNOLOGY

After studying different techniques, we came to know that the techniques in the previous paper are more complex. So, we prefer GDI (Gate diffusion Input) as our proposed technology.

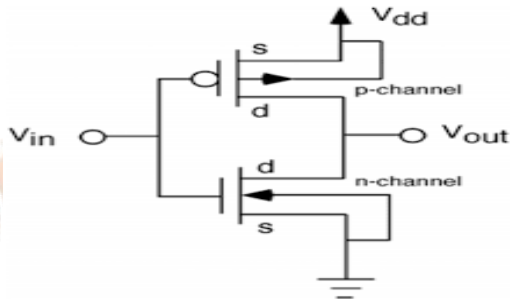

Fig. 2: CMOS Inverter

The GDI cell is similar to the CMOS inverter logic.In CMOS inverter, the source of PMOS is connected to VDD and the source of NMOS is grounded. The GDI cell has three inputs: the first case of GDI input is G-common input, which is connected to the gate of PMOS and NMOS, and the second case of GDI input is N-input, which is connected to the source or drain of PMOS, and the third case of GDI input is P-input, which is connected to the source or drain of PMOS. The major difference between CMOS and GDI is that GDI has N, P and G terminals that would be given as a supply voltage, VDD, or grounded or they could be supplied as an input signal depending on the circuit we design.

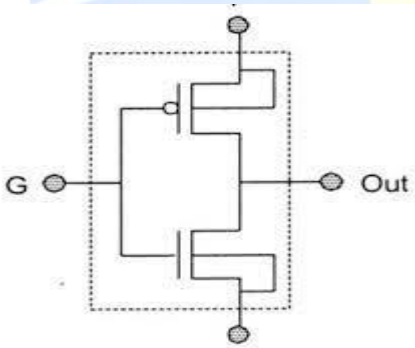

Fig .3: GDI Cell

So, we are using 10 transistors to implement a full adder using this technique. When compared to the CMOS full adder, which requires 54 transistors to built an adder.

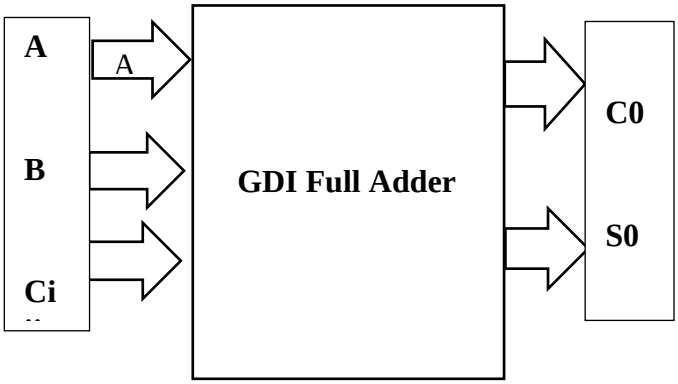

Fig .4: Block diagram for GDI Full Adder

Table 1: Truth table for Full Adder

Inputs			Outputs	
A	**B**	**Ci**	**S0**	**C0**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	0	1	1

Table 2: Logic Function For GDI Cell

N	P	G	OUT	GATE
0	1	A	$\bar{A}$	NOT
B	0	A	AB	AND
1	B	A	A+B	OR
$\bar{B}$	B	A	$\bar{A}B+\bar{B}A$	XOR
B	$\bar{B}$	A	$AB+\bar{A}\bar{B}$	XNOR

IV. FUTURE WORK

In the future, some work can be done to get a high speed, low power full adder implemented by using the Ripple Carry Adder (RCA) or Carry Look ahead Adder (CLA).

V . RESULTS AND SIMULATION

In this section the performance of the Effectual adder using the GDI techniqueis evaluated using the cadence virtuoso tool at 45nm CMOS technology. The Full adder Efficiency is given in terms of power consumption. The Sum and Carry are in terms of volts and the power in terms of nano watts. The full adder is implemented using XOR, AND, and OR gates in logic style. The following figure 5 shows the GDI Full adder schematic using the cadence tool.

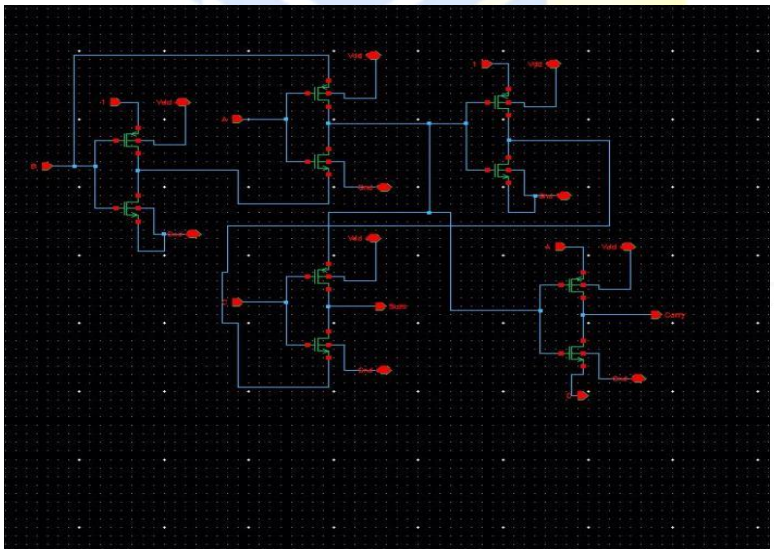

Fig .5: Schematic Diagram for GDI Full Adder

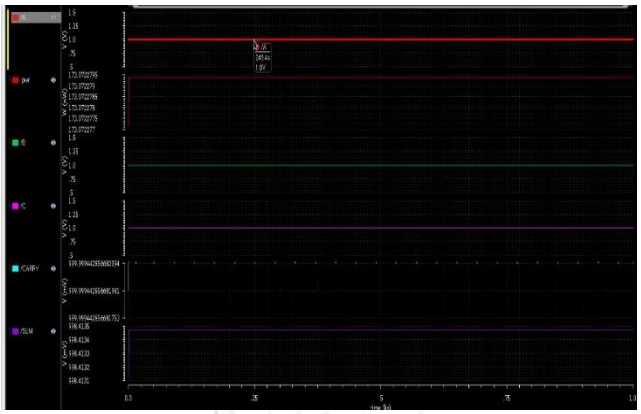

Fig. 6: power results for GDI Full Adder

VI. COMPARISON OF DIFFERENT LOGIC STYLES

The Logic styles generally dependon power consumption, area,and speed.The below table shows the comparison of different logic styles:

Table 3: Comparison of different logical techniques

Logic style	Power (µw)	Delay(ns)	Number of transistors
CMOS	65	1.94	54
DPL	119	2.03	48
CPL	97	1.17	32
GDI	0.168	0.01	10

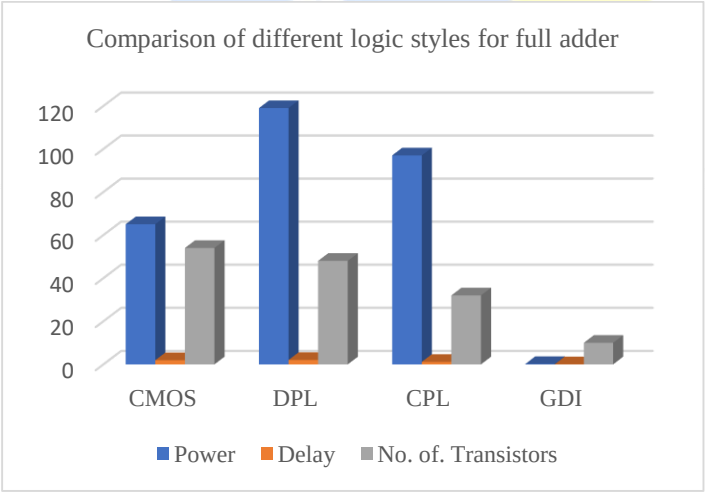

FIG.7.COMPARSION OF DIFFERENT TECHNIQUE

The power consumption of the GDI full adder is reduced by 25% when compared to CMOS adder

VII. CONCLUSION

The design of a low power, effective adder using GDI has been presented with great results using the Cadence Virtuoso tool on records of power consumption for the proposed adder when compared to the previously published realisations.

The full adder designed using GDI logic with very low power consumption of around 100 to 400 nanowatts which is very low power consumption to achieve the high performance of the Adder.

VIII. REFERENCES

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