Three - Bit Low Power Encoder Using Memristor

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Abstract —The design of digital logic gates using a memristor gives an alternative to the present IC design. This will be one among the upcoming Computing Architecture. The manufacturing of MRL gates is simple because memristor can be designed on top of the polysilicon gate of NMOS transistor. There will be an increase in density of transistors on a chip. The Proposed 3-bit Encoder design using MRL dissipates low Power as compared with CMOS design. This device is used to model different combinational logic circuits and this paper mainly aims to design and analysis of a 3-bit encoder with different logics using LT spice

Index Terms - Memristor, Pseudo NMOS logic, CMOS logic, Combinational circuits, Encoder.

I. INTRODUCTION (HEADING 1)

In the era of big data, data protection is vital and challenging because no one can predict where and when the next downtime will occur. Data backup technology is one of the best solutions in practice to minimize data loss and other negative impacts. Therefore, the efficiency in data backup and restoring will determine whether the system can maintain a continuous and stable operation. During the backup process, data stored in the volatile memory will be transferred to the nonvolatile memory and restored after downtime ends. The latency for the data transportation mainly depends on the type of memory and the structure of the system. How to minimize such latency becomes crucial for the efficiency of data backup.

Memristor (abbreviation of "memory resistor") is one of such emerging memories. It was predicted by Leo Chua in 1971 [1] and coined by HP lab in 2008 [2]. This passive device has been explored to have multiple advantages such as nonvolatile, high density, low power consumption, high integration, and good compatibility with CMOS devices. It has also been discovered that the use of memristors in memory components enables the volatile memory to store its intermediate states with high speed at a low cost.

So far, to design electronic circuits, passive elements like as capacitors, resistors, and inductors are used, but a fourth fundamental element also exists, which is called a "memristor".

Memristance is simply charge-dependent resistance and the unit of the memristor is the ohm.

As a hypothetical non-linear passive two-terminal electrical component, the concept of memristor was first proposed based on the perspective of the circuit integrity [1]. Memristor has the notable nonvolatility property of having the memory of how much electric charge has flowed and in which direction through it in the recent past, which determines its present resistance. When the electric power supply is turned off, the memristor remembers its most recent resistance until the power is turned on again. This property can then be exploited to build a nonvolatile memory component. Since the first practical memristor model was built by HP Labs [2], many other models have been proposed to characterize the electrical characteristics of memristors in terms of voltage, current, and state variables in different application scenarios. A detailed description of these models can be found in an ISQED survey [8].

II. LITERATURE SURVEY

L. Chua, "Memristor-The missing circuit element," in IEEE Transactions on Circuit Theory, vol. 18, no. 5, pp. 507-519, September 1971, doi: 10.1109/TCT.1971.1083337.

A new two-terminal circuit element-called the memristor characterized by a relationship between the charge and the flux-linkage is introduced as the fourth basic circuit element. An electromagnetic field interpretation of this relationship in terms of a quasi-static expansion of Maxwell's equations is presented. Many circuit-theoretic properties of memistors are derived. It is shown that this element exhibits some peculiar behavior different from that exhibited by resistors, inductors, or capacitors. These properties lead to a number of unique applications which cannot be realized with RLC networks alone. Although a physical memristor device without internal power supply has not yet been discovered, operational laboratory models have been built with the help of active circuits. Experimental results are presented to demonstrate the properties and potential applications of memristors.

Liu, Gongzhi & Shen, Shuhang & Jin, Peipei & Wang, Guangyi & Liang, Yan. (2021). Design of Memristor-Based Combinational Logic Circuits. Circuits, Systems, and Signal Processing. 40. 1-22. 10.1007/s00034-021-01770-1.

This paper proposes three modified memristor ratioed logic (MRL) gates: NOT, NOR and A AND (NOR B) (i.e., $A \cdot \bar{B}$), each of which only needs 1 memristor and 1 NMOS. Based on the modified MRL gates, we design some combinational logic circuits, including 1-bit comparator, 3-bit binary encoder, 3-bit binary decoder and 4:1 multiplexer. Furthermore, an improved multifunctional logic module is proposed, which contains one NMOS transistor and five memristors, and can implement AND, OR and XOR logic operations. Using this multifunctional logic module, a 4-bit comparator and a 1-bit full adder are designed.

Memristor based XNOR for high speed area efficient 1-bit Full Adder

In this paper nano-device property of Memristor has been utilized to design an area efficient high speed full adder. In comparison to other design of logic gate and full adder, the novel full adder circuit has the advantage of simplified architecture, better speed and higher power efficiency. The adder comprises of only 15 NMOS transistors and 15 Memristors. The prime philosophy of the work is to provide a Memristor-based solution for designing the alternative Computation-In-Memory architecture and effective extension of Moore's Law.

S. Kvatinsky, G. Satat, N. Wald, E. G. Friedman, A. Kolodny, and U. C. Weiser, "Memristor-based material implication (imply) logic: Design principles and methodologies," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 22, no. 10, pp. 2054–2066, 2013. An IMPLY logic gate is a natural way to perform logic operations with memristors. This logic gate can be integrated within a memristor-based memory and, together with FALSE, provide a complete logic family. This memristive logic gate also enables non-von Neumann architectures, which may open a new era in computer architecture. The potential benefits of memristive circuits in terms of density and power support further work in this field. The results described in this paper can be used to direct further research on device structure optimization, logic synthesis methods, array structures, and computing architectures.

III.IMPLEMENTATION

Information in digital logic circuits with specific meaning is encoded into corresponding binary bits. Encoder is a circuit which does this encoding function. The encoder's function is to encode when one of the input bits is of effective level, and the encoder's output changes in accordance with its input bits. The circuit has 'N' outputs and 'M' inputs and they are related by M = 2N .

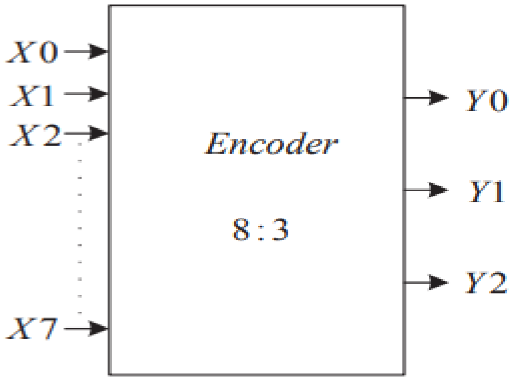
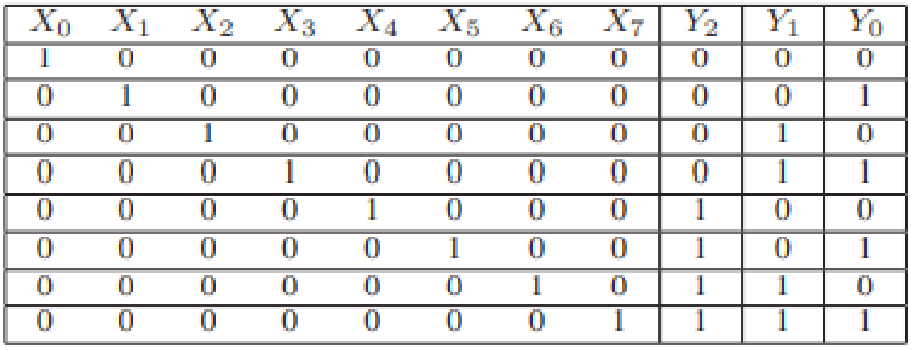


Fig: 3-bit encoder



X_0	X_1	X_2	X_3	X_4	X_5	X_6	X_7	Y_2	Y_1	Y_0
1	0	0	0	0	0	0	0	0	0	0
0	1	0	0	0	0	0	0	0	0	1
0	0	1	0	0	0	0	0	0	1	0
0	0	0	1	0	0	0	0	0	1	1
0	0	0	0	1	0	0	0	1	0	0
0	0	0	0	0	1	0	0	1	0	1
0	0	0	0	0	0	1	0	1	1	0
0	0	0	0	0	0	0	1	1	1	1

Fig: Truth table encoder

From the Encoder truth table, the outputs and inputs are related by

Y0 = X1 + X3 + X5 + X7

Y1 = X2 + X3 + X6 + X7

Y2 = X4 + X5 + X6 + X7

From these relations, logic circuit can be implemented using CMOS, Pseudo NMOS and MRL. In the Encoder circuits, X1- X7 are input bits and Y2, Y1, Y0 are output bits. In Encoder circuit by using MRL, M1, M2, M3, M4 act as pull-down network and a Memristor acts as pull-up network. M1, M2, M3, M4 and Memristor constitute a 4-input NOR gate. X1, X3, X5, X7 are the input signals that pass through the NOR gate and the signal at the drain of M1 is inverted signal of (X1 + X3 + X5 + X7). M13 and Memristor constitute an inverter. The output of 4-input NOR gate is given as the input of inverter. The signal at the drain of M13 is Y0 = X1 + X3 + X5 + X7.

PROPOSED SYSTEM :-

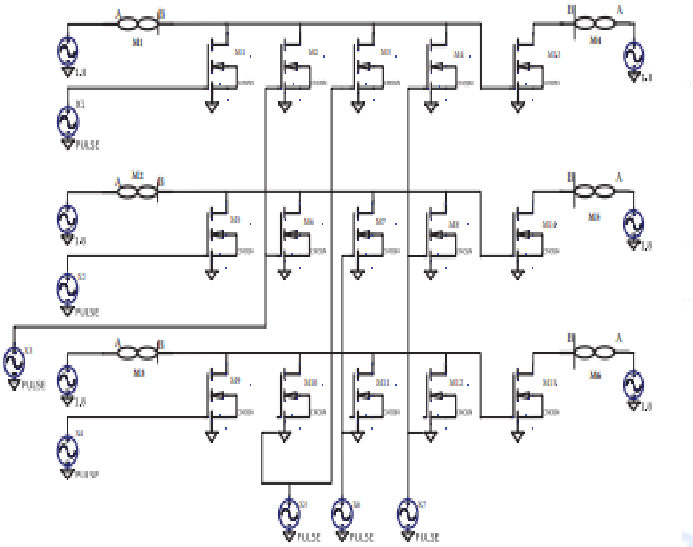


Fig: Schematic of encoder using memristor based logic

EXISTING SYSTEM : -

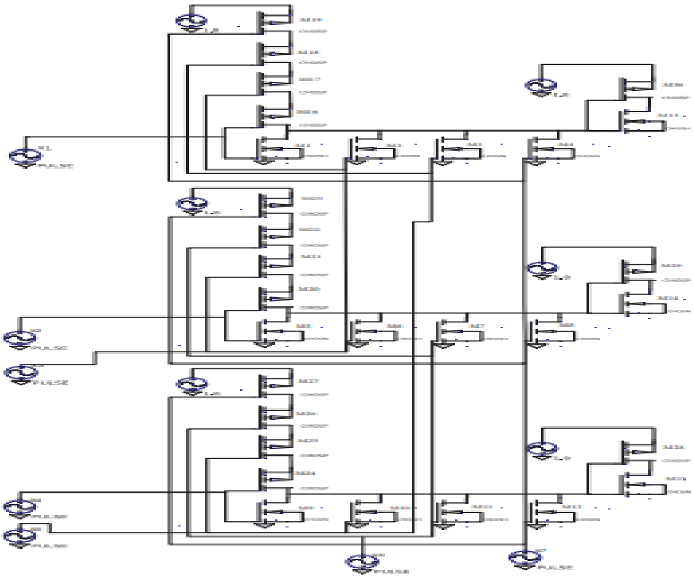


Fig: Schematic of encoder using CMOS Logic

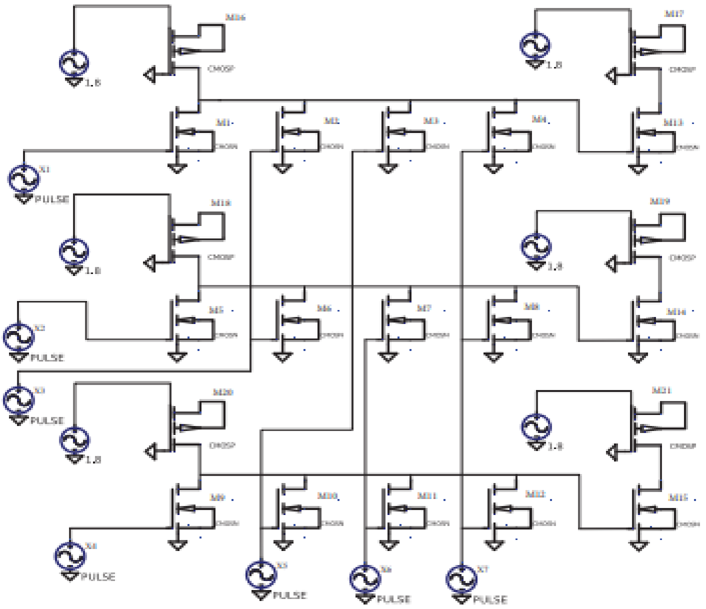
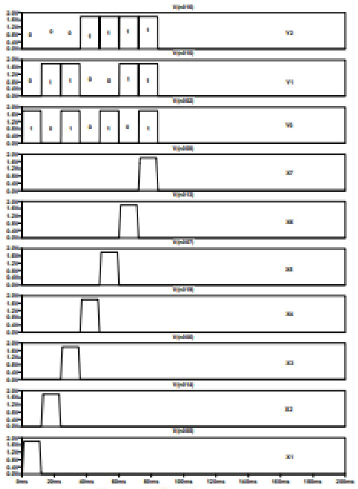


Fig: Schematic of encoder using PSEUDONMOS Logic

As, it is known that the area occupied by a Memristor based design is lesser than CMOS [11], [14], [15], it can be depicted that this design is efficient with respect to the area consumed. It can be seen that the number of transistors that are required for this design is the least when compared to the conventional CMOS and Pseudo NMOS logic. By using CMOS technology, the encoder circuit has 30 transistors, of which 15 PMOS and 15 NMOS. By using Pseudo NMOS technology, the encoder circuit has 21 transistors, of which 5 PMOS and 15 NMOS. By using MRL technology, the encoder has 21 transistors, of which 6 Memristors and 15 NMOS.

OUTPUT WAVE FORMS



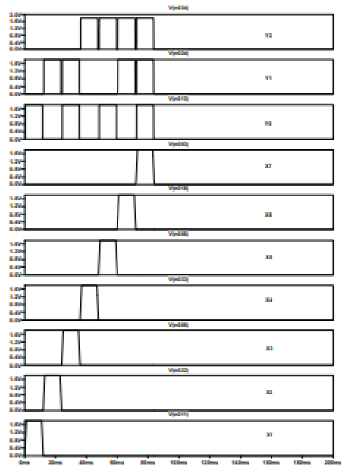


Fig. 11. Output of encoder using CMOS

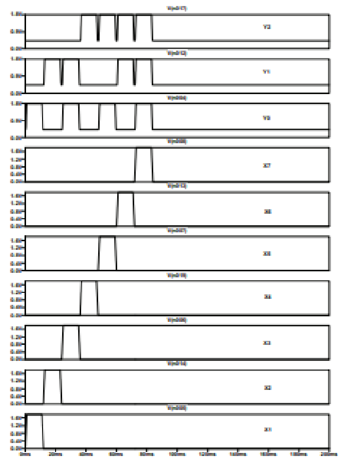


Fig. 14. Output of encoder using Pseudo NMOS

Comparison of performance parameters among CMOS, Pseudo NMOS and MRL based encoders.

	Average power	*Delay*
CMOS based encoder	12.94µW	154.083ps
Pseudo NMOS encoder	149.93µW	77.5194ps
MRL based encoder	2.563µW	77.0416ps

III. CONCLUSIONS

Design of encoder with Memristor based logic design is much efficient in the aspects of power and area when compared with conventional CMOS logic and Pseudo NMOS logic. The trade-off between the power, area and speed of a circuit is persistent. It can be concluded that this design technique gives lesser number of transistor count required and makes it more efficient way of designing a digital circuit.

IV. REFERENCES

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