Low Power Priority Encoder Design using LT Spice

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Abstract - Encoder is a combinational circuit which executes the opposite operation of decoder. It converts the binary datas into N-output lines. Priority encoder is one of the major type of encoder but the only difference is that it gives the outputs on the basis of highest prioritized inputs. By using simple logical circuit the output power is consumed 0.154 but by using CMOS priority encoder circuit the output power is tremendously reduced by 99%. In case of logic gates output power 1,2 & 3 are 158 mW and for CMOS priority encoder circuit output power 1 = 1.768 µW, output power 2 = 1.3 µW and output power 3 = 1.43 µW.

Index Terms - CMOS, Priority Encoder, Power Reduction, 4-bit, LT Spice

I. INTRODUCTION

Encoder is a combinational circuit which executes the opposite operation of decoder. It converts the binary datas into N-output lines. Priority encoder is one of the major type of encoder but the only difference is that it gives the outputs on the basis of highest prioritized inputs. In this paper, 8 to 3-bit CMOS priority encoder is used in LT Spice simulator. A 8 to 3-bit priority encoder is implemented at 5 V CMOS technology to calculate the low power consumption. As compared to the conventional Designs More than 40% of power consumption, speed is improved by 57% , area is reduced by 5%, transistor count is reduced to 35%, total power dissipation of 77.1% and the improved delay of 36%. But no any work has been done till now for low power in electronic devices using python language. So in this to calculate the low power in CMOS encoder circuit by python language using LT Spice simulator has been done.

II. LITERATURE SURVEY

Xuan-Thuan Nguyen et al.[1]The two well planned architecture of 64 bits and 256 bits priority encoder using 1D to 2D array conversion methods are displayed and executed Silicon on thin buried oxide of 65-nm CMOS process. Because of the high performance and low power design, the SOTB CMOS process is used. As results at 1.2 V be seem that manufactured PE256 chip was operated at 45 MHZ and consumed at 291 W approximately. The leakage power was reduced at 0.6 V in sleep mode. **Won Namgoong and Teresa H. Meng[2]** A designed real-power PVQ encoder that absorbs 2.1 MW for compacting 256 x 256 pixels per frame seqences of videos at 30 frames per sec in 0.8 microns at CMOS technology. The strategy of algorithm design which is hardware driven was taken to provide extra pipelining and parallelism in thye architecture with the dimensions of 256. T5his is the way for reaching high compression efficiency which maintain the quality of image at the low levels of power. **Shao-Wei Huang and Yen-Jen Chang[3]** The full parallel priority encoder is used in comparator circuit. The execution of full parallel priority encoder is way better than the conventional priority encoder. The 90nm CMOS technology is applied in comparator with full parallel priority encoder. As a results showed that the designed proposed is 12% and 40% more faster than NAND-type priority encoder based comparator. Comparator is based on parallel MSB. The critical path becomes shorter by using full parallel priority encoder which improvise to differentiate performance efficiently. **Reza Hashemian[4]** High speed compact priority encoder is enlarges for Parallel operation with high density. The CMOS technique which is high and simply efficient is executed for the establishment of priority resolution modules. A staircase array structure based technique is used as an array to reduce the hardware. Due to this parallel operation causes in the modules inside the same level. Also the scheme of pre-charge or pre-discharge is used for the reduction in time response if that modules. A dense, fast ans new priority encoder is built for 32-bit data. Design is simulated on CMOS technology for 2.5 microns. **Jose G. Delgado-Frias[5]** The scheme of priority encoder and CMOS design are introduced. To decrease the prioritry propagation delays, a novel priority lookahead scheme is used. The approaches of two priority encoder are introduced one with PL scheme and other is without PL scheme. The VLSI encoder of 32-bit with PL scheme which is about to reduce the time by 2.5 times of output than the other encoder. The two dynamic circuits are designed and developed for the implementation of the priority encoder. The technology used for encoder schemes are 1-micro meter SCMOS and 32-bit priority encoder. **Miad Faezipour and Mehrdad Nouani[6]** The introduction of low power and high speed multi match priority encoder design which is applicable in many networking systems and computers. The scalable multi-match prioritizer logic circuit is proposed which can find

the first r coordinated inputs from the set. The data partitioning scheme is used to recognise input data efficiently for the improvement in the performance. The technology of 0.18 micro meter is used for implementing VLSI to achieve speed. More than 40% of power consumption is reduced to small piece of TCAM cells. **Jinn-Shyan Wang and Chun-Shing Huang[7]** The structured designed of high speed priority encoder is introduced. Mainly the idea of multi level look ahead structure is designed expertly by CMOS logic of single phase clocked dynamically. To calculate the performance, 3-V 0.6 micro meter CMOS technology is implemented on 32 bit priority encoder. As comparision between the conventional and the new designs, speed is improved by 57% and area is reduced by 5%. **Saleh Abdel-hafeez and Shadi Harb[8]** A designed priority encoder with high performance using CMOS standard library cell is introduced. The scheme is tried to minimize the whole propagation delay between the evaluated low and high priority logic circuits. The introduced encoder shows improvement in speed, modularity and routing as compared to the pre-existing designs of encoders. 32- bit priority encoder is used for the improvements and 0.15 nu-m TSMC CMOS technology is used in this process. As a results the 32-bit encoder is operated at its maximum frequency of 667-MHz with 1106 transistors and 13.3 mW of maximum power consumption. **J. Aishvarya et al. [9]** The designed novelity of recursive systematic convolution encoder is introduced using the reversible gates. The RSC encoder is coded in HDL language of Verilog and integrated in 90 nm DC tool library. This encoder is designed by using reversible logic gates which achieve the notable improvement as compared to the conventional designs in respect of power dissipation. As compared to the simple logic gates the reversible logic gates consumes less power. **Maksuda Rabeya et al.[10]**Nowadays, CMOS technology is facing some problems which can be resolved by nano technology based quantum dot cellular automata. The less power is consumed and and low power devices can be created by this technology which allows to design digital logic circuits. The design of priority encoder and 4 to 2 encoder can used as 3 dot based architechture of QCA. The design was simulated and the compared with the pre-existing designs which results it has reduced number of cells and also consume less area. **Chung-Hsun Huang et al.[11]** Lookahead signals are used for the formation of multi-level folded architecture to improvise the performance of O(log N). The incrementer or decrementer and priority encoders logic functions are much the same thatswhy that can designed by the similar techniques. According to the analysis both multilevel folding and multilevel lookahead techniques could easily combined and executed in dynamic CMOS circuit. The consumption of power at its maximum frequency is reduced to 67% and the count of transistors of incrementer or decrementer is reduced to 35% when compared with design based on CSA. The introduced 64-bit incrementer or decrementer and 256-bit priority encoder are operated upto 116 and 139 MHz and designed on 0.6 nu-m CMOS technology**. Satendra Kumar Maurya and Lawrence T. Clark[12]**The designed low power circuits priority encoder is designed with compact and high speed by using CMOS gates is introduced. Comparing with the implementation of dynamic domino circuit the power and delay has been improved. The approach of 8-bit priority encoder circuit shows power dissipation of 77.1%, transistor count of 63.6% and the improved delay of 36%. **Dimitrios Balobas and Nikos Konofaos[13]**The 256-bit CMOS priority encoder is designed with efficient energy and high performance using 32-nm technology. The new full custom circuit is designed which includes dynamic inversion technique and multiple-output monotonic CMOS technique. And when it comes to comparision with convensional design, the new circuit is improved in delay of 57%, consumption of energy by 8% and EDP is improved by 39%. The 32-nm technology is used which can do the circuit more compact, fast and energy efficient than 256-bit conventional designs. **Jinn-Shyan Wang and Chung-Hsun Huang[14]**The two techniques are used for high speed i.e., multilevel look ahead structure to develop a short critical path and NP Domino CMOS logic which are connected parallelly in circuit structure. The circuit structure is connected in series for low power and high speed at the same time to decrease the activity of switching. To calculate the feasibility many priority encoders of 32-bit are designed in 3 V 0.6 n-m CMOS Technology. In the new designed structure it gets improvement of speed by 65%, area is reduced by 30% and power is reduced by 30% in the comparision with conventional designs. **Anirudh Raghunath and Shikha Bathla[15]**The involvement of gadgets acquires loss power in the electronic industries. The CMOS technology is very famous for low power electronic gadgets. After three years, the transistors counts used per chips will increased and by scaling the measurements of gadgets, leakage current increased. Multiple techniques for the reduction of power are used i.e., LECTOR, DTMOS etc. **S. Samanta,et al.[16]** Clocking scheme is used in flipflops to the era of digital system which helps to search the circuit's load output which called as clock load. The switching circuit is pretentious by clock load. Power waste of circuit in its sleeping mode are low in flip-flops. **Biswarup Mukherjee and Anirudda Ghosal[17]** The performance of this device fully depends on temperature which switch fastly with high power consumption. CAD tool seems of 35% reduction after simulation in power consumption as compared to the conventional designs. **Michaelraj Kingston Roberts[18]**The modified variation of ripple carry adder of N-bit with high speed and low power is proposed. The two 14-transistors added cells are the new technique which secondly repeated as the substitute of identical

adder cell. The power is maintained when constituents number is decreased in critical path. The complexity problem is distinguished by the performance of high speed. **Pranay Singh and Promod Kumar Jain[19]**NOR gate is used in designing of circuit which help in high speed designing and low power designing. The total count of transistors reduced from 166 to 116 which used to reduce the consumption of power and circuit delay. **Rahul Shrestha[20]**The carry-look ahead adder is pipelined the critical path to compose the logic gates. To decrease the power consumption inexact-spectulation adder architechture been clock-gated. The platform of FPGA used to verify the function and implement the hardware. The previous simulation of 32-bit ISA is done CMOS technology by 90 nm for the examine of power and area. **Robert Giterman et al.[21]** The balanced 8T SRAM cell which consists of two transistors to reduce the leakage current. The upgraded security if memory array is shown for the cells were carry out in CMOS Technique of 65-nm. The secured data is holded by 6T SRAM macros. **Zhao Zhang et al.[22]**To keep the constant loop bandwidth a loop bandwidth-tracking technology is taken to make LVHDPLL work robustly over temperature variation, process and voltage.To save the comsumption clock frequency should be dynamically controlled for gated source switched charge pump and digiotal loop filter. PLL is the clock module in SOCs so, it is very useful for the designing and implemention of low power and low voltage PLL. **Lei Wang et al.[23]** A low power generator of forward and reverse biased with biased switches to put the voltage dynamically. To reach low power comsumption in load current of range o-30 mu, reverse body bias generator of P-well which uses pulsated frequency modulation bases power converter with switching capacitor. For configuration of FRBB generated voltage dynamically BB switch is to be make known. **Xizhu Peng et al.[24]**A low power and low cost of on-chip digital background calibration algorithm decreases the noise effect and also can be applied for various stages. It inhances the accuracy of the calibration . It can be easily executed with low hardware cost and less power on chips. **Hayate Okuhara et al.[25]** Method to optimize power which improves the performance or power control and get analysed with processor chips. Power Optimization is based on delay and power model to reduce complexity. **Ki-Chan Woo et al.[26]**By replacement of the D flip-flops both unidirectional and bidirectional latch-based thermometer-code shift registers reduces the power consumption and area. **Haoyu Zhuang et al[27]**Edge-race comparator differentiates differential input voltage by calculating the distance between two edges and by generating the two propagating edges in two inverter loops. The comparator is a low power which can adjust its power comsumption easily. **Ivan Ratkovic et al.[28]** Clock-gating technique is comprehensively evaluated for vector FMA units. This technique is evaluated by using application based on both synthetic and real-world. Power is saved by using vector instruction-based clock-gating techniques.

III. METHODOLOGY

The 4:2 priority encoder circuit of four inputs and two outputs is constructed which includes three or gates, one and gate and one not gate. A voltage supply is given to every input supply of 5v and the values of transient analysis is given which is 160m. the resistance of 5v is given before output to measure the power analysis of the circuit. As a results, after simulation the output power is measured at Vout and the graph is obtained which has low power as compared to the previous convensional designs.

IV. RESULTS

In the result the simulation of 4:2 priority encoder circuit has been done in LT Spice and graphs are obtained at different inputs. Firstly logical diagram of 4:2 encoder circuit has been simulated in LT Spice at 5 volts and output voltage and current are obtained and with the help of the results power has been calculated. Secondly 4:2 cmos encoder circuit has been simulated at 5 volts and the output voltage and currents are obtained and then the power has been calculated. As a results, by comparing the logical priority encoder with cmos priority encoder, the power is tremendously reduced in cmos priority encoder.

V. FIGURES AND TABLE

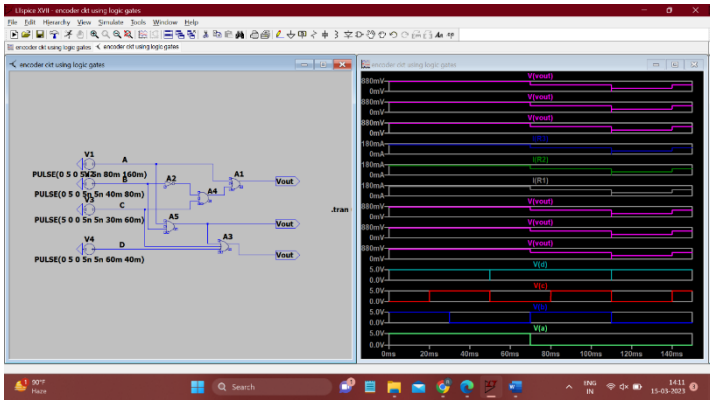

Fig.1 Logical Priority Encoder Circuit

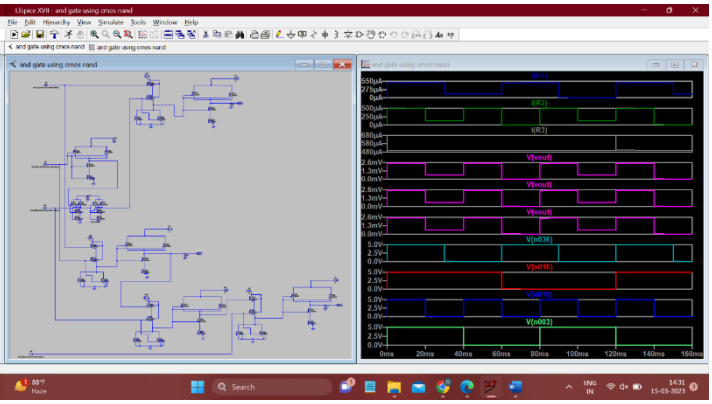

Fig.2 Logical CMOS Priority Circuit

TABLE:

	Logical Priority Encoder Circuit			CMOS Priority Encoder Circuit			
Outputs	Voltage (V)	Current (Amp)	Power (W)	Voltage (V)	Current (Amp)	Power (W)	Power Saved (Δ)
Output 1	880 mv	180 mA	0.1584 W	2.6 mv	680 µ amp	0.000001768 W	0.9993 W
Output 2	880 mv	180 mA	0.1584 W	2.6 mv	500 µ amp	0.0000013 W	0.9999 W
Output 3	880 mv	180 mA	0.1584 W	2.6 mv	550 µ amp	0.00000143 W	0.9999 W

VI. EQUATIONS

P = V*I
Where, P = Power (Watt)
V = Voltage (Volt)
I = Current (Ampere)

Δ = (ΔW % W)%ΔW
Where, ΔW = Power of CMOS Priority Encoder Circuit
W = Power of Priority Encoder Circuit.

VII. CONCLUSIONS

This paper reviews the 4:2 priority encoder circuit and conducts further graphical analysis on a 5V CMOS Technology. The measurement results are at 5V. The power is reduced and calculated with the help of resistance connected before output. A 4 to 2-bit priority encoder is implemented at 5v CMOS technology to calculate the low power consumption. As a result, after simulation the graph is obtained at 5v.

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