Physical Design Implementation of MIPS Processor in 28nm Technology

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Abstract – The layout assembly and connecting of digital logic gates in accordance with the design input file (also known as the netlist) of an integrated device, such as a processor, while adhering to design criteria like as timing, power, and area are referred to as physical implementation. We used the synthesis team's contributions in this design, and the physical design flow from import design, floor plan onward placement, and signoff was done using the physical design tools. At each stage, time (hold and setup), report quality, congestion, routing, and other parameters are scrutinised.

***Key Words*: Import Design, Floor Plan, Placement, Place opt, Clock Tree Synthesis, Opt Clock Tree Synthesis, Routing, opt Routing, Signoff.**

1.INTRODUCTION

To guarantee the physical architecture of the MIPS processor satisfies the requirements of functionality and speed, constraints were generated from the design netlist, which includes information on the cells employed, their interconnections, area, and other parameters. Before moving on to the next level, we did some preliminary floor planning to determine the ideal aspect ratio and core area.

Using the available macros as a guide, we strategically positioned them to maximise use and prevent bottlenecks in later phases. After the chip was divided into smaller blocks for power and layout design, all wire load models (WLM) were eliminated because placement relied on RC values from VR to determine timing. Prior to, during, and following placement optimization, placement was performed. After CTS, the insertion latency is reduced by clock tree synthesis by balancing the skew. After performing routing, which is split into global and detailed levels, we go on to search and repair, and finally, the cells do ECO checks including timing ECO, functional ECO, metal ECO, power ECO, and clock ECO. Physical verification is performed after the other physical design phases have been completed to ensure that the resulting layout design is accurate. Examples of these include the design rule check (DRC), layout vs. schematic (LVS), antenna vs. rule check (ARC), and error rate check (ERC) (electrical rule checking). Finally, we have a firm grasp of the database file format used as the gold standard in the industry for data replacement of IC layout artwork—the Graphic Database System (GDS II) file. It's a binary file that represents a layout's hierarchy of geometric objects on a flat plane, as well as any text labels or other information that might be needed to describe the layout.

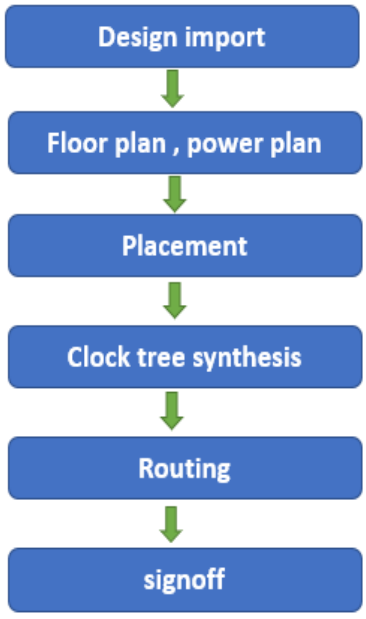


Fig -1: Physical Design Flow

1.1 DESIGN SPECIFICATIONS

- Technology node: 28nm
- Layers: 9 Routing metal Layers
- Macro counts: 38
- No. of Clocks: 9 Clocks
- Total Cells: 0.60 Million
- Target clock Frequency: 500 MHz
- Voltage Domain: 1

2. IMPORT DESIGN

Import design is the first step in Physical Design. At this stage, all required inputs and essential references are interpreted into the tool, and primary checks, such as design and technological consistency, are performed.

2.1 Inputs Required in Import Design

Gate level netlist, logical (timing) and physical views of all other IPs utilised in the design, timing constraints (SDC), power intent (UPF), scan DEF, technology file, and RC Coefficient files are all required inputs.

2.2 Sanity Checks

Sanity checks scan through the concerns related to library files, timing limitations, IOs, and optimization directives. In terms of time, they effectively check the condition of the netlist. Sanity checks that have been done include the following

1. Library checks: to see if any duplicate cells are present or not, as well as missing pin information and cell information.

report_design_mismatch

2. To check for combinational loops, empty modules, inputs with floating pins, nets with tristate drivers, nets with multiple drivers, Declare assignments

report_netlist

3. Input and output delays and unconstraint pathways should not be present to verify that all flops are clocking.

report_timing

3. FLOORPLAN

This is the first big step in finishing the layout. Your chip quality is determined by your floor layout here. We define the size of your chip/block, allocate power routing resources, place the hard macros, and reserve space for standard cells during this phase. A good floorplan can make the implementation method (place, CTS, route, and timing closure) a piece of cake. Similarly, a poor floorplan can cause a slew of problems in the design (congestion, timing, noise, IR, routing issues). A faulty floorplan will increase the area, power, and damage the reliability and life of the IC, as well as raise the overall IC cost (more work to close, more LVTs/ULVTs).

3.1 Deciding the Utilization factor & aspect ratio

Aspect ratio will decide the size and shape of the chip. It is the ratio between horizontal routing resources to vertical routing resources (or) ratio of height and width.

Aspect ratio = width/height

Core utilization:- The area occupied by standard cells, macros, and additional cells will be defined by utilisation. If the core usage is 0.8 (80%), it signifies that 80% of the core space is used for standard cells, macros, and other cells, while the remaining 20% is used for routing.

core utilization = area of (macros + std cell +pads)/ total core area

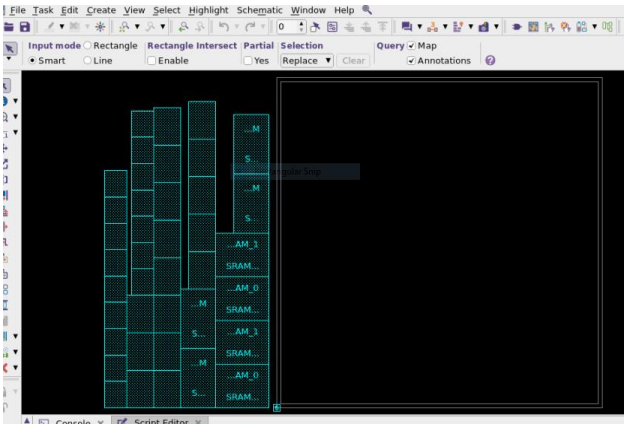


Fig 1.Creation of core and die area

After creating core and die area will go for legal placement of pins.

3.2 port placement

Pin constraints can be set by specifying sides,allowed layers,pin spacing,corner keepout distance.

Then by using command, place_pins the placement of pins is done.

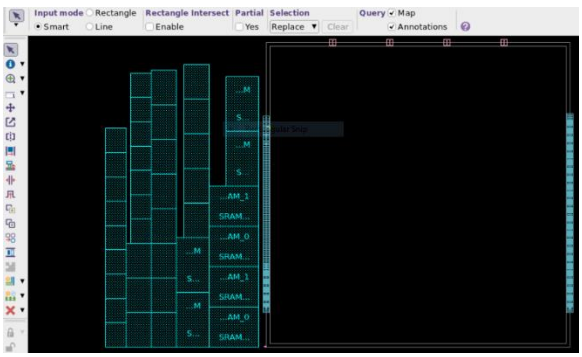


Fig 2. Port placement

3.3 Macro placement

After placement of ports next step will be the placement of macros.

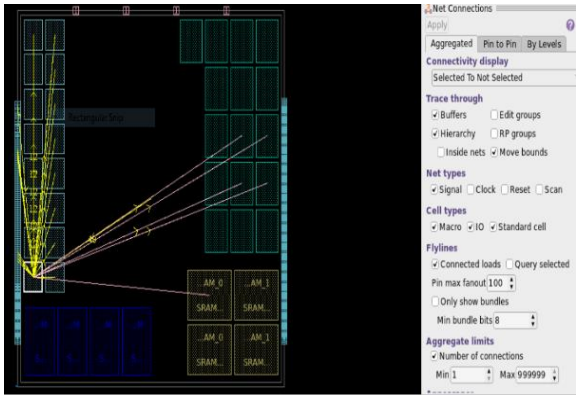


Fig 3. Macro placement according to dataflow connectivity

- Place macros based on their families
- Decide macro location based on flyline analysis
- Place macros by performing macro to macro analysis
- Avoid placement of macros near ports in order to avoid congestion in later stages
- Place halos around macros to avoid congestion around macros
- There should be gap between macros
- Put blockages between macros
- Avoid notches while placement of macros

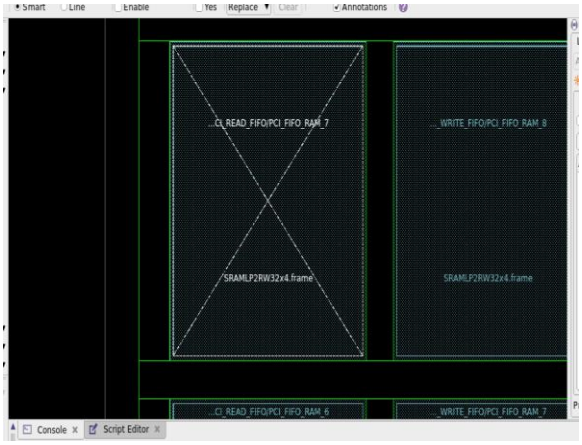


Fig 4. Creation of keepout margin and blockages

3.4 Physical cells

The physical cells such as end cap cells and tap cells will be placed,end cap cells will be used to avoid manufacturability issues for standard cells placed near to boundary.so,near to boundaries rather than standard cells end cap cells will be placed.Tap cells will be placed at instant of places to avoid the latch up issue for standard cells.

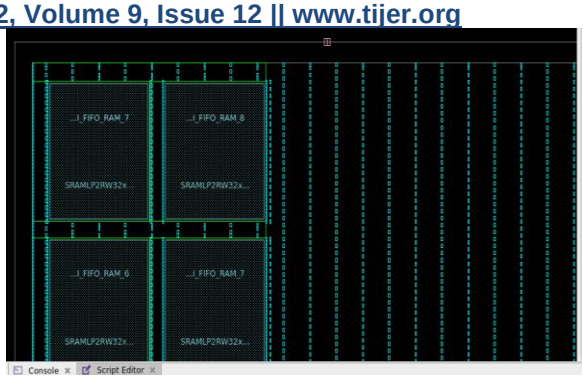


Fig 5.Insertion of Boundary cells and tap cells

3.5 Powerplan

After placement of preplaced cells the next step is power distribution. Power need to be distributed uniformly throughout the core area. It will be distributed in such a way from power ports to straps and from straps to rails and from rails to standard cells. The metals will be connected through vias.

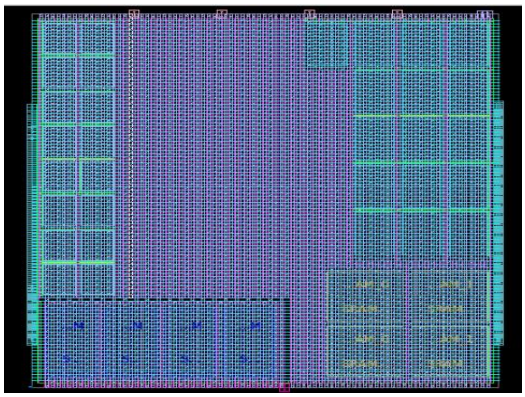


Fig 6.After powerplan

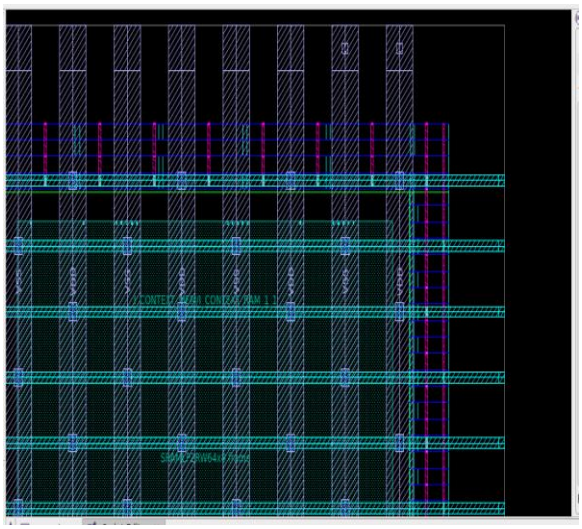


Fig 7. Power distribution through metal layers

Checks to be done,

1.check pg connectivity
2.check pg drc's
3.check legality
4.site row orientation
5.pin overlaps

4.PLACEMENT

It is a process of placing all the standard cells which are present in design.

It going to be done in 5 steps

Place opt

1. initial_place
2. initial_drc
3. initial_opt
4. final_place
5. final_opt

In first step, tool going to place according to timing and if buffer aware means add more no. of buffers and will do scan chain re-ordering. In second step it will remove extra buffers added and will do high fan-out net synthesis. Data path optimizations will be done in third step. In fourth step w.r.t timing and congestion optimizations will be done. scan chain reordering and legalization will be done in the last step.

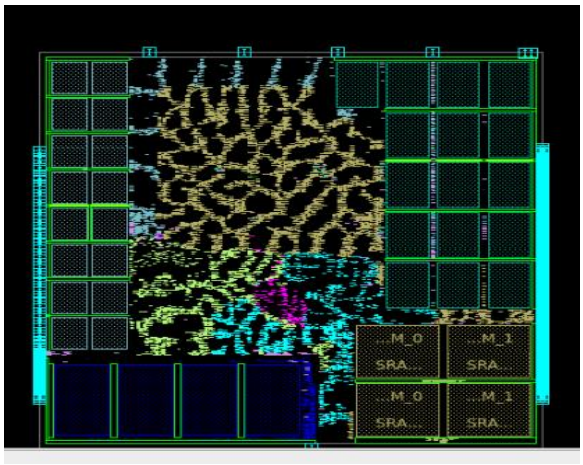


Fig 8.placement of standard cells

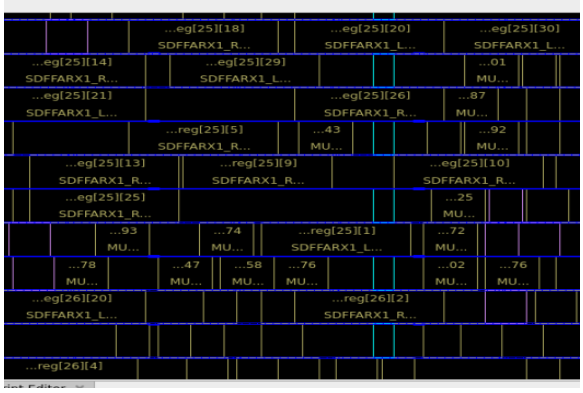


Fig 9.standard cells in design

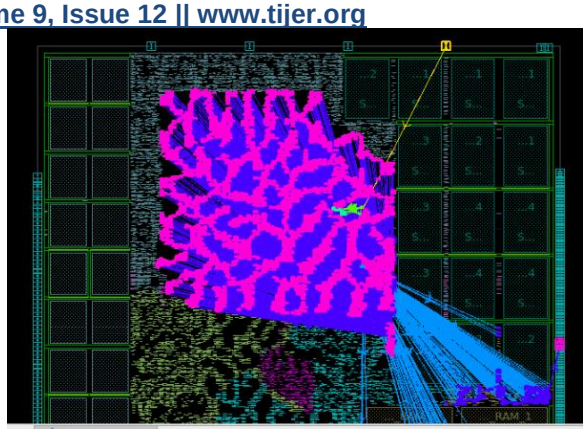


Fig 10.Ideal clock propagation in placement

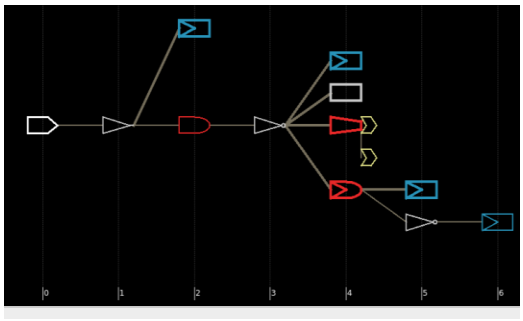


Fig 11.clock structure in placement stage

Checks,

1. Congestion
2. Legality
3. Timing
4. DRV'S

5.CLOCK TREE SYNTHESIS

In this process clock going to be distributed to all the sequential cells which are present in the design.

Clock_opt

CTS will be done in three steps

1. clock building
2. clock routing
3. post cts optimizations

For clock building it will use different types of tree but in our design it has used fishbone for clock distribution.According to the transition value specified in cts specification file tool takes those value and place clock buffers or inverters at instant of nets.some of nets having more insertion delay need to balance the skew by considering global skew specified in cts specification file tool going to balance skew by increase of min id or by decrease of max id.

Checks,

1.congestion
2.timing
3.drv's
4.skew
5.clock qor

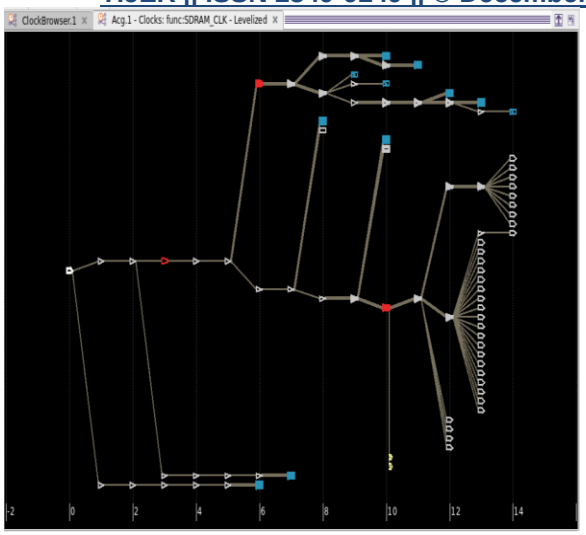


Fig 12.clock structure in CTS

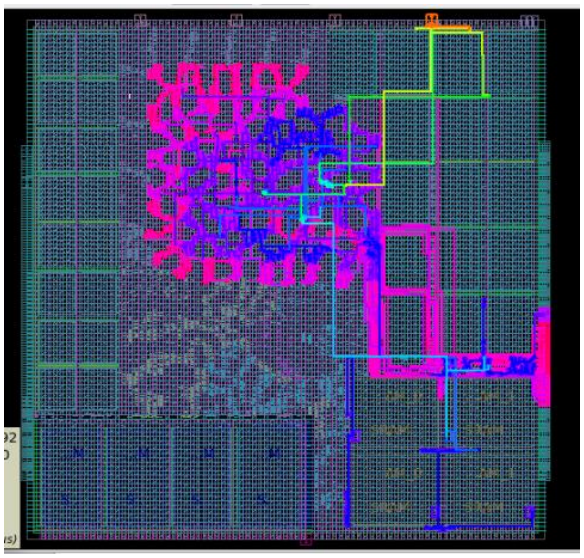


Fig 13.clock propagation in CTS

6.ROUTING

It is process of distributing signal to all the cells which are present in the design.
It will be done in 4 steps

1.global routing
2.track assignment
3.detail routing
4.search and repair

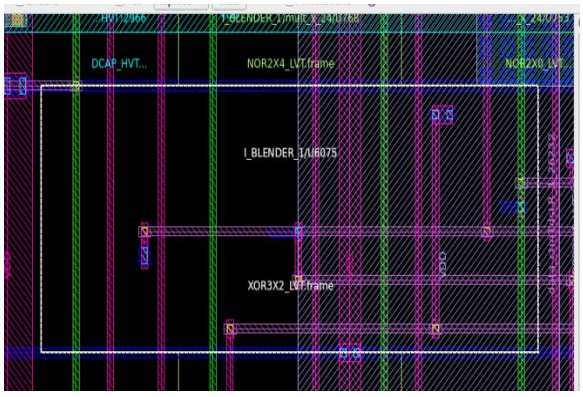


Fig 13. Signal nets in routing

RESULTS :

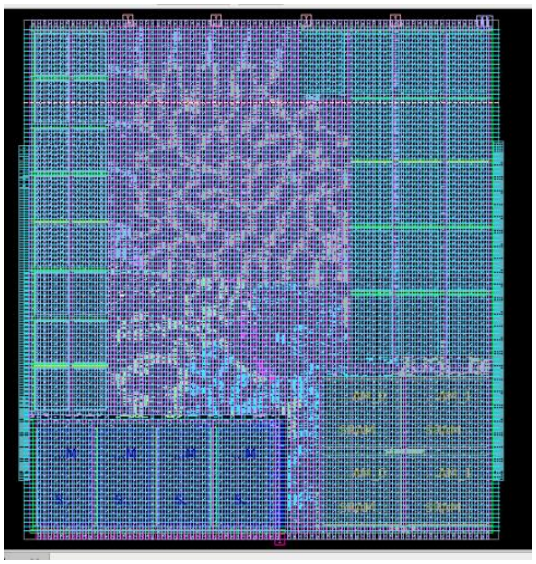


Fig 14. Final result after placement and routing

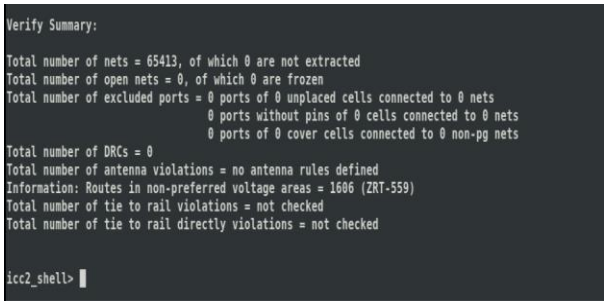
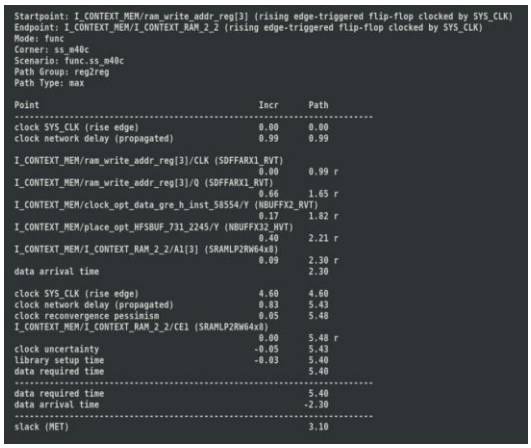


Fig 15. Clean with DRC'S



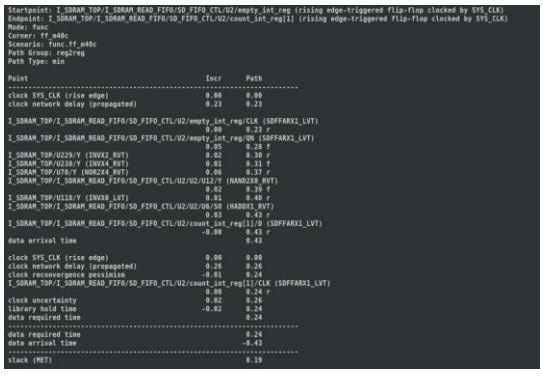


Fig 16.Timings(setup &hold) met

7.CONCLUSION

By passing each and every quality check during the floorplan, placement, clock tree synthesis, and routing, the MIPS processor's physical architecture is implemented. CTS used to match the statistical analysis's skew, duty cycle, delay, pulse width, and clock tree power and the design is clean with respect to drc's and timing(setup,hold) violations

REFERENCES

1. Kahng A, Lienig J, Markov I, Hu J. VLSI physical design: From graph partitioning to timing closure. Springer, 2011, 27.
2. Mehrotra, Alok, Van Ginneken, Lukas P, Trivedi, Yatin. Design flow and methodology for 50M gate ASIC, IEEE Conference Publications, 2003.
3. Y. Li, A. Farshidi, L. Behjat, and W. Swartz. High performance post-placement length estimation techniques. International Journal of Information and Computer Science, 1(6):144–152, September 2012.
4. D. O. Ouma, D. S. Boning, J. E. Chung, W. G. Easter, V. Saxena, S. Misra, and A. Crevasse. Characterization and modeling of oxide chemical-mechanical polishing using planarization length and pattern density concepts. IEEE Transactions.
5. PHYSICAL DESIGN ESSENTIALS - An ASIC Design Implementation PerspectiveKhosrow Golshan.