Literature Survey of Low Power Strategies and Comparative Analysis of 28nm Technology Node in VLSI Physical Design

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***Abstract*— In 28nm CMOS technology, device power characteristics drastically change. Low power is one of major concerns in modern VLSI design as the technology scales, we have faster and smaller devices. Low-power design principles are essential due to the complexity of contemporary applications and deep-submicron technologies. Potential savings increase with design abstraction level, increasing as abstraction increases.. This study has analysed and compared a number of prior low power designs, including clock gating, power gating, multiple supply voltage designs, and dynamic voltage/frequency scaling (DVFS) and PWM Pulse Width Modulation Low-leakage Biasing techniques.**

***Keywords*— low power, 28nm technology, clock gating, low power, power dissipation, SoC, PWM, DVFS, power gating**

I. INTRODUCTION

Low power is one of the main considerations to be concerned about in every VLSI circuit. The building blocks used in smart grid technology perform specific independent duties that have been allocated to them in the form of algorithms that have been put into the appropriate circuits where power needs are meant to be reduced. Each of these algorithms will be composed of a distinct circuit utilizing flip-flops and gates. From this point on, any circuit is constructed using VLSI as a foundation. Area, power, and timing are only a few of the variables that impact VLSI design. Every VLSI chip design is now significantly impacted by power dissipation and management. There is a growing demand for smaller, more portable electronic devices as the speed, mobility, and downsizing of present electronic products rise. One of the important requirements during a design process is to know how much power the circuit should dissipate, considering its application. Both static and dynamic

II. SOURCES OF POWER DISSIPATION

There are four sources of power consumption in digital CMOS circuits – dynamic, static, short-circuit, and leakage:

$$P_{total} = P_{dynamic} + P_{static} + P_{short} + P_{leakage} \quad \text{.....(1)}$$

A. *Short-Circuit Dissipation*

A small amount of current flows through both the PMOS and NMOS during the switching operation. This current has no effect on recharging the load capacitor (C load). As a result, this current is referred to as short circuit current.

B. *Leakage Dissipation*

In both active and standby modes, leakage energy is lost**.** Sub-threshold leakage (ISUB), gate leakage (IGATE), gate induce drain (IGIDL), reverse bias junction leakage (IRB) are the four primary components.

$$I_{leak}=ISUB+IGATE+IGIDL+IRB\text{.....(2)}$$

C. *Static Power Dissipation*

This type of power dissipation is the most prevalent one seen in digital circuitry.

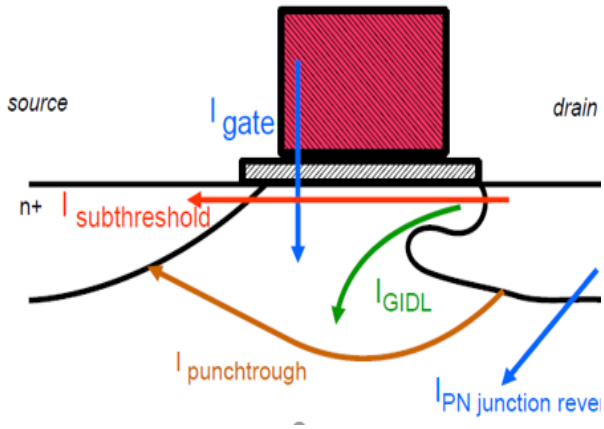

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Fig 1: Cmos Leakage Mechanism

D. *Dynamic Power Dissipation*

The most efficient method for reducing dynamic power is the reduction in supply voltage caused by technology scaling, which lowers threshold voltage. Leakage currents, gate tunneling currents, and leakage power in standby mode increase under deep submicron technology as the threshold voltage is reduced. Leakage current and leakage power dissipation are both caused by the majority of portable devices' prolonged standby modes.

$$P_{dynamic} = C \cdot {V_{dd}}^2 \cdot \alpha \cdot f \text{.....(2)}$$

III. BRIEF LITERATURE SURVEY OF EXISTING LOW POWER TECHNIQUES

CLOCK GATING:

Clock gating technique's main goal is to stop circuits from receiving unwanted clock pulses when there won't be any change in the output. According to the circuit design, the and this will only be enabled when they reach a logic 0 or 1 value. This causes a decrease in area and power. The first step in implementing clock gating is to identify the ideal location to employ the approach to reduce overall power usage and to develop logic for that location to control when the clock enabling signal is turned on and off. When a particular flip-flop or register is idle, that unit is blocked and does not require a clock pulse. This condition is described by the term "clock enabling signal. "The main cause of the dynamic power loss is a shift in the flip-flops' transition state between 0 and 1 [5]. Reducing the flip flop's switching activity slows down the change in state, progressively shrinking the area as a result. Therefore, the straightforward solution is to stop the inactive clock pulses for those circuits in sequential circuits. This lowers the amount of power used, which also reduces the amount of space needed.

POWERGATING: When the design is dormant, power-gating is a particularly efficient method for reducing SOC design leakage power. However, with deep sub-micron technologies, idle blocks greatly increase power consumption and create huge leakage currents. a definite a proactive approach to end this standby, Power-gating is the consumption of power. While a design uses power-gating, sleep transistors are positioned between the power supplies and the logic cells as switches to turn off the power when the design is not in use. Due to its great leaky reduction efficiency in sleep mode, power-gating technology has been frequently used in lithium ion systems to extend battery life.. In 28nm CMOS SOC designs, this has changed as a result of two serious problems. First, the power density of the 28 nm node is getting close to the point where it could, if not controlled, lead to silicon failure. Second, leakage power must be reduced as it has overtaken other sources of chip power in 28nm devices.

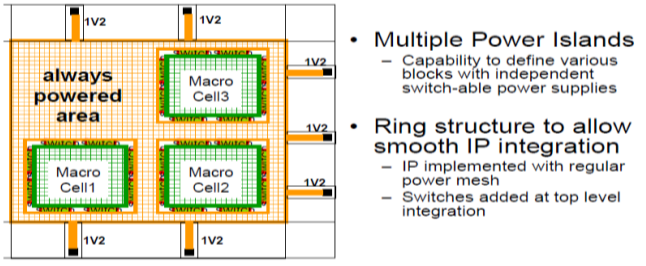


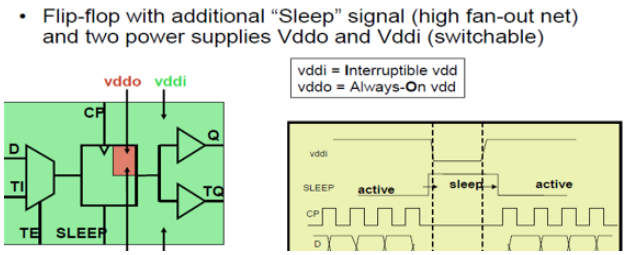
Fig 2: POWER GATING + RETENTION FLIP FLOPS

Types based on power gating

a. Selective state retention Power Gating
b. Power gating with body biasing
c. Sub clock power gating

state retention Power Gating

The power consumption of the SRPG design area are greatly reduced by this selective SRPG technique .The primary premise of the SSRPG technique is that ordinary designs should finish all outstanding calculations before entering a non-active state rather than needing to apply PG at every potential stage. A subset of the e-FFs necessary for the right state retention can be chosen by restricting the range of states



the design's power gateable threshold. All other FFs are classified as not absolutely necessary FFs (n-FFs) in terms of state retention because they do not need to be kept around. The following two criteria are used to determine which e-FFs should be included in the design in order to apply the approach described in this study.

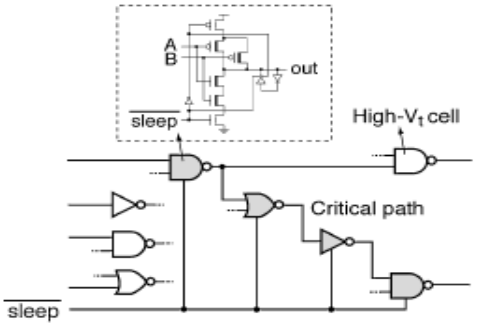


Fig 3: Selective Power Gating

DRAWBACK:

owing to the additional retention memory cells, the fundamental drawback of the SRPG technique is its large area over head , which is 40 to 60% higher than that of PG. The backend implementation complexity and standby power consumption are further increased by the excessive addition of retention memory cells compared to PG.

Power Gating with Body Biasing

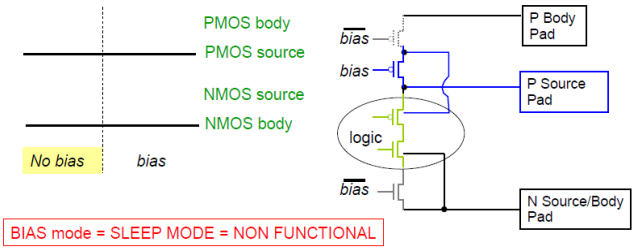
In this circuit, however, a body-bias generator is linked to the pMOS devices' (n-well) bodies. The forward body bias (FBB), which is applied while the header is in active mode and the generator is applying a voltage less than Vdd, causes the pMOS devices to run more quickly by decreasing their Vt. The reverse body bias (RBB), which is applied in sleep mode when the header is off at a voltage greater than Vdd, increases the Vt of the pMOS transistors and decreases leakage.

a) Requires low current drive
b) Requires Voltage higher than VDD for PMOS (easy: IO)
c) Requires Voltage lower than ground for NMOS (uneasy)

BIASING

d) Requires high drive current (uneasy)
e) Both needed off-chip voltage control or on-chip

BIASING EXAMPLE (without bias):



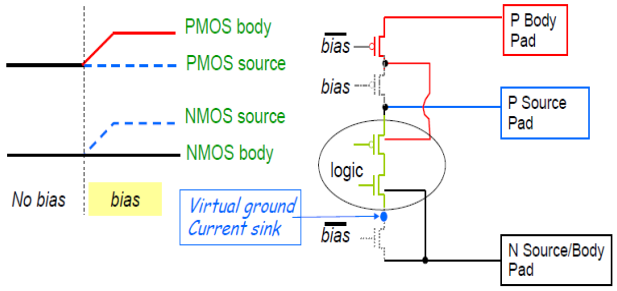
- Low on-resistance, PMOS source direct to pad
- Source bias for NMOSs and body Bias for PMOS

From Intel, Clark *et al.* « Reverse body bias and supply collapse for low effective standby power» VLSI 2004

BIASING

i. Limit
   a. Breakdown voltage of gate oxide
   b. Rise in VGB gate Leakage currents

ii. Benefit
   c. rise in Vth, reduces PN junction and leaky power



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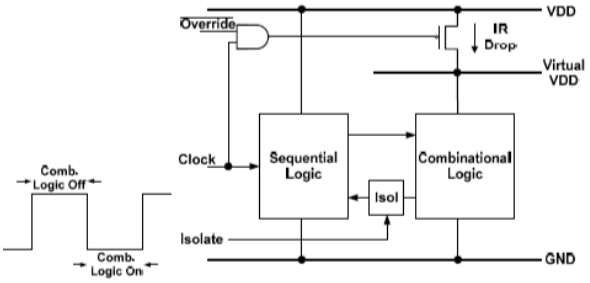
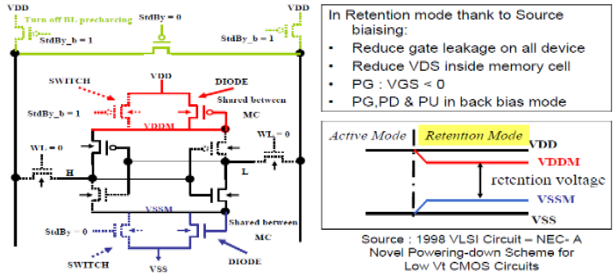


Fig 5: Sub clock power gating technique

BIASING EXAMPLE (with bias):

SOURCE BAISING ON SRAM



DVFS:

Each power domain's voltage and frequency are dynamically scaled in accordance with its own performance need, which is determined by the FIFO's occupancy level. The domain output is transferred to the following pipeline stage by being buffered in the FIFO. Additionally, the power management unit (PMU) that supplies each domain with a clock and supply voltage is governed by this performance requirement. It is recognised as a method to lower the power and energy consumption of microprocessors to use dynamic voltage frequency scaling (DVFS) . only reducing the operating

The energy consumption can be decreased with frequency fclk, but it stays the same because the computation takes longer to complete.

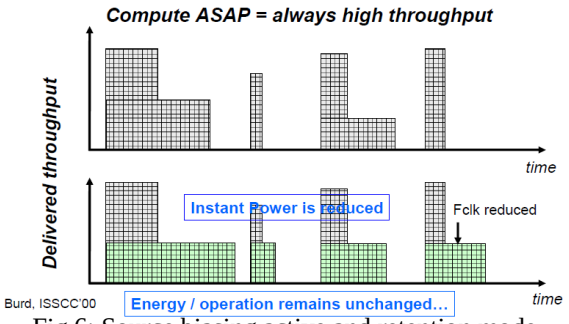
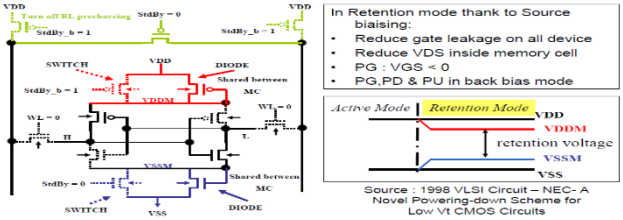
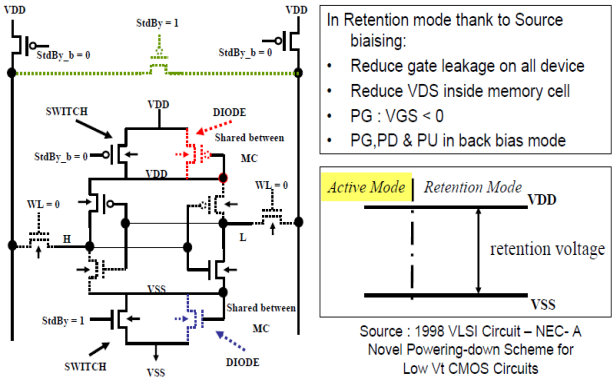


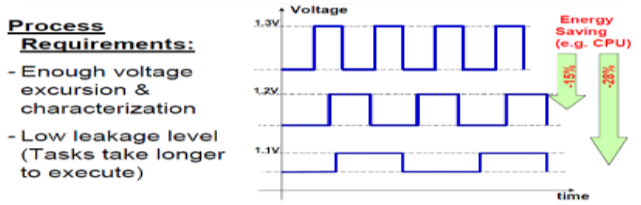
Fig 6: Source biasing active and retention mode



Scaling the frequency to complete operations on time:



DYNAMIC VOLTAGE & FREQUENCY SCALING :



DYNAMIC POWER REDUCTION THROGH HW-SW INTERACTION:

IV. Conclusion

This paper proposes a framework for the analysis of low power techniques' energy efficiency. For high-quality production designs, the 28nm CMOS technology's two most pressing problems—power and process variations—must be fixed. With mains-supplied SOC designs, the power-gating method is now applicable. Multi-Voltage is crucial for stable production SOC designs.. Power-critical design of twenty eigt nanometer SOC raises concerns about the always-on nwell biasing technique, which is frequently employed in power-gating design.

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