Designing of an ASIC block level Physical design Implementation of I²C Protocol on 40nm Technology

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Abstract—ASIC Block level physical design implementation is process of transforming netlist into layout (GDSII) without worrying about functionality. The process of generating the layout of an ASIC from a GLN using a software tool is called automatic place and route. The goal is to design a layout such that it meets the design goals such as performance, power and area(PPA). This study has a top-down approach as its technique. The steps used to realize a layout are design and timing setup, sanity checks, Floor plan and powerplan, Routing, synthesis of a clock tree, and placement of standard cells, signoff. Automatic place and route is performed by using icc2 tool.

Keywords—design and timing setup, sanity checks,I²C protocol , floorplan, powerplan, Routing, synthesis of a clock tree, and placement of standard cells , signoff.

I . INTRODUCTION

One of the crucial steps in the Application Specific Integrated Circuit (ASIC) flow, sometimes referred to as the backend design flow, is physical design. In contrast to general purpose integrated circuits, application specific integrated circuits are chips created to carry out a specific set of tasks. ASIC'S can be implemented using different design flows depending on the circuit size,design complexity and number of parts required.A library of standard cells and macros are used as primitives in the ASIC design flow hence this flow is also referred to as the semi-custom design flow.VLSI designs can be realized much quicker using the ASIC design flow when compared to the full custom design flow.ASIC design flow has evolved to handle very large and complex designs.It can handle speeds and meet low power requirements when compared to FPGAs.Implement an ASIC design presents many challenges due to the following high feature count,Need for high performance,Time to market pressure.In physical design flow Load the required libraries technology files, Sanity tests primarily examine the temporal accuracy of the netlist. Floor planning is the technique used to establish zones for standard cell placement using the tool and decide the location of macro cells and IOs, powerplanning is the process of adding metal wires to connect power pins of all macros and standard cells to the external source while meeting the IR drop goal , The placement is the process of automatically inserting standard cells in rows produced by floorplan so that it complies with the temporal restrictions provided in the SDC ,The process of connecting clock pins of all sequential cells to the clock net such that clock skew is minimized is called clock tree synthesis(CTS),The process of creating metal connections (traces)between pins of all the cells in a design in accordance with gate level netlist(GLN) while meeting DRC,LVS and timing constraints is called routing.

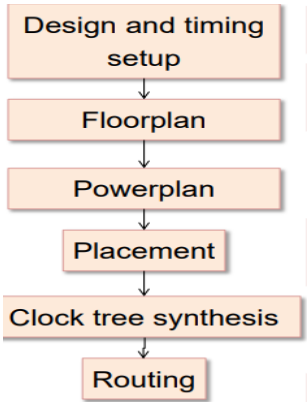


Fig -1: Physical Design Flow

1.1 Design Specifications

- Technology: 40nm
- Layers:7
- Macros count:34
- Instance count:38887
- Supply voltage: 1.1V
- Vt of transistors: svt, lvt, hvt
- Area(approximate):4.2mm²
- Clock frequency:833MHz
- Power consumption:600mW
- Max.IR drop(VDD+VSS):5%

II. Design and Timing setup

A. The PnR tool is loaded with the information from the following input files.

- *Netlist (.v/ .vhd/ .edif)*
- Physical Libraries (.lef)
- Timing Libraries (.lib)
- Technology Files
- Constraints (.sdc)
- IO Info. File (optional)
- Power Spec. File (optional)
- Optimization Directives (optional)
- Clock Tree Spec. File (optional at floorplan stage)
- DEF/ FP (optional if floorplan is not done)

B. Core area is approximately calculated by the tool from the Netlist

C. While Importing, first we have to load the LEF files and then LIB files

II. SANITY CHECKS

Sanity Checks primarily examines the timeliness of the netlist's quality.

Additionally, it involves looking at problems with library files, timing constraints, IOs, and optimization directives.

1. Library checks
   i. Missing cell information
   ii. Missing pin information
   iii. Duplicate cells
2. Design checks
   iv. Inputs with floating pins
   v. Nets with tri-state drivers
   vi. Nets with multiple drivers
   vii. Combinational loops
   viii. Empty modules
   ix. Assign statements
3. Constraint checks
   x. All flops are clocked or not
   xi. There should not be unconstraint paths
   xii. Input and output delays.

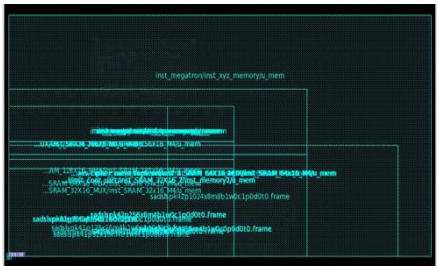


Fig 2: Imported design

III . FLOOR PLAN

Floorplanning is the process used to define the die area, determine the placement of macros and IOs, define regions for standard cell placement, define standard cell rows. In block level floorplan automatic place and route (APR) uses a hierarchical flow to minimize design time and hardware requirements, design is broken into smaller blocks. This process is called design partition. Each blocks runs through automatic place and route called block level APR flow. Block level refers to the floorplan of a block of a design. Block level floorplan involve placement of macros

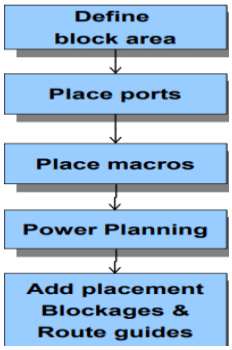


Fig-3: Block level floorplan

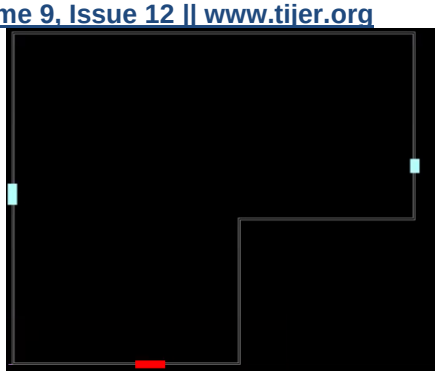


Fig 4: Core Area, Die area,IO ports Defined

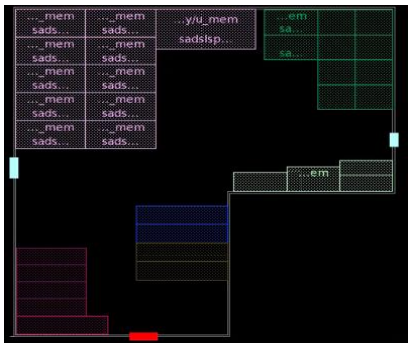


Fig 5: Macros placed

IV.POWER PLAN

Power planning is the process of adding metal wires to connect power pins of all macros and standard cells to the external power source while achieving the EM and IR drop objectives. calculating the size, distance, and quantity of power nets (example: VDD and VSS) nets on the layout. Power network must meet IR drop goal, typically 5% of supply voltage.

a) Power plan: IR drop

IR drop analysis generates IR drop maps to enable the designers to check if IR drop goals are met. Inputs required layout of the design with power network, current drawn by each cell in the design, resistance estimation tables for the technology used for manufacturing the design.

b) Power plan: Electro migration (EM)

Electro migration the process of gradual displacement of metal atoms of a route in an IC due to the high density that causes the metal ions to drift in the direction of current flow. It results in opens or shorts of metal routes, it happens over time. The solution is to reduce the current density by increasing the metal width, Electro migration rules specify maximum current density for a given width to the route.

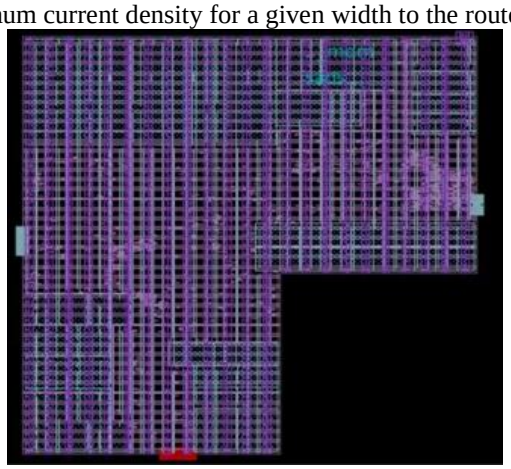


Fig 6: Power plan & IR drop

V. STANDARD CELL PLACEMENT

In order to fulfil design restrictions like time, area, and power, standard cells are automatically placed in standard cell rows that were formed during the floorplan process. It is an iterative process, how well a design meets its constraints in placement depends on the floorplan.

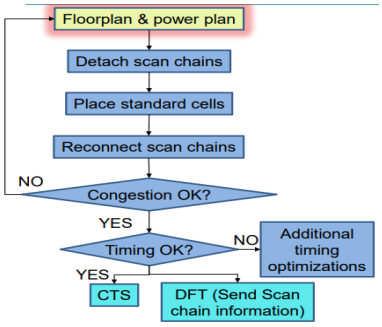


Fig-7: Standard cell placement flow

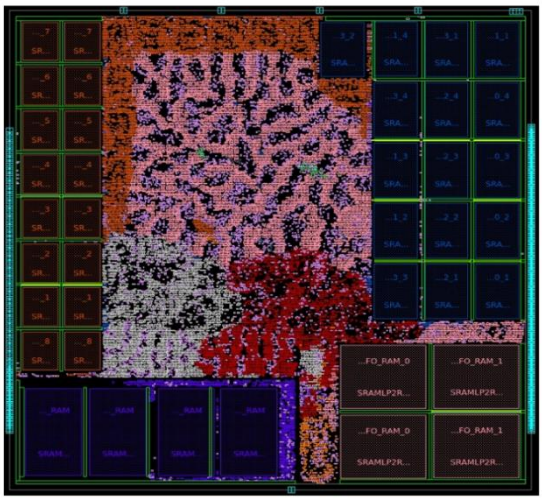
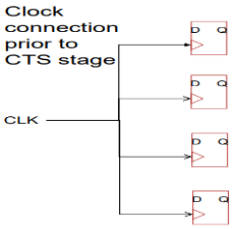


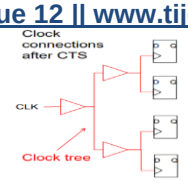
Fig-8: standared cells placed

VI. Clock tree synthesis (CTS)

The process of connecting clock pins of all sequential cells to the clock net such that clock skew is minimized is called clock tree synthesis (CTS). Synchronous designs use clock to synchronize data between sequential elements typically the clock nets connect to a large number(>million) of sequential cells. Clock nets are treated as ideal during clock tree synthesis. Interconnect delays from the layout will degrade the quality of the clock signal and introduce delays, resulting in clock reaching the flip-flops at different times(skew)causing timing violations. Ideally the clock skew must be zero clock skew affects setup and hold time of a timing path. Clock tree synthesis adds buffers and/or inverters is called a clock tree.



Before clock tree synthesis



After clock tree synthesis

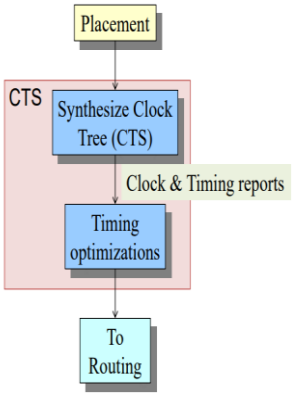


Fig 9: Clock tree synthesis flow (CTS)

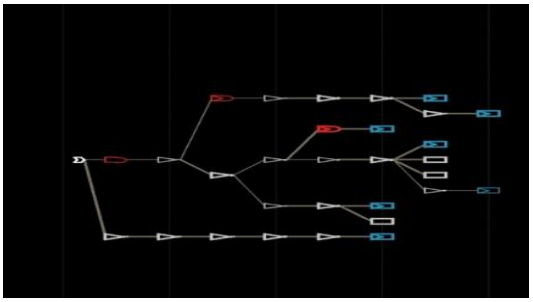
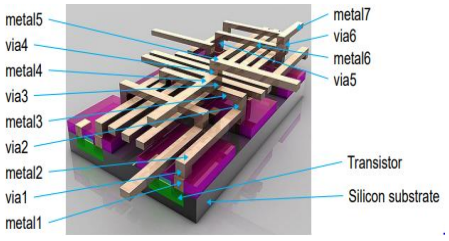


Fig- 10: Clock tree built

VII. ROUTING

The process of creating metal connections (traces) between pins of all the cells in a design in accordance with gate level netlist(GLN) while meeting DRC,LVS and timing constraints is called routing. Multiple metal layers maybe used to route a net. Multiple layers are typically called metal,metal2 and so on. Alternate metal layers are routed in opposite directions,vias are used to connect alternate metal layers.



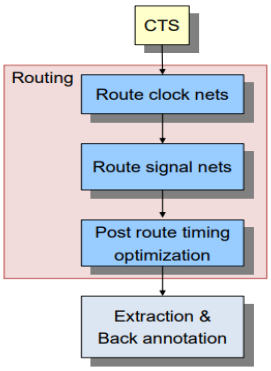


Fig 11: Routing flow

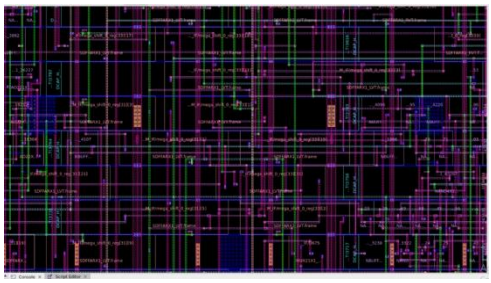


Fig 12: Routing stage

VIII. SIGNOFF

Electrical rule check (ERC), layout versus schematic (LVS), and antenna check are carried out at signoff. In order to assure effective fabrication, design rule check (DRC) is the process of comparing physical layout data to foundry-specified rules. Verifying a verilog netlist's connection using layout versus schematic (LVS) (Extracted netlist from GDS) An IC design's electrical connection is examined or verified using the Electrical Rule Check (ERC) method. Maximum net length restriction when linked to the gate terminal during antenna inspection (Gate-oxide integrity check).

IX. CONCLUSION

By passing each and every quality check during floorplan, power plan, standard cell placement, clock tree synthesis, routing, and signoff, as well as clock tree synthesis to meet latency, skew, duty cycle, pulse width, and the clock tree power compared with the statistical analysis, the I2C protocol is implemented at the ASIC block level physically. It has no DRC,LVS, or DFM concerns. It complies with the IR drop goal and has no timing or LEC faults. It has never violated setup, hold, or slew rules. To guarantee that the design is completed by prime time and the icc2 tool and meets the necessary criteria and timeliness, an engineering change order (ECO) is made.

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